

Extending SDN and NFV with Deep Data-Plane Programmability

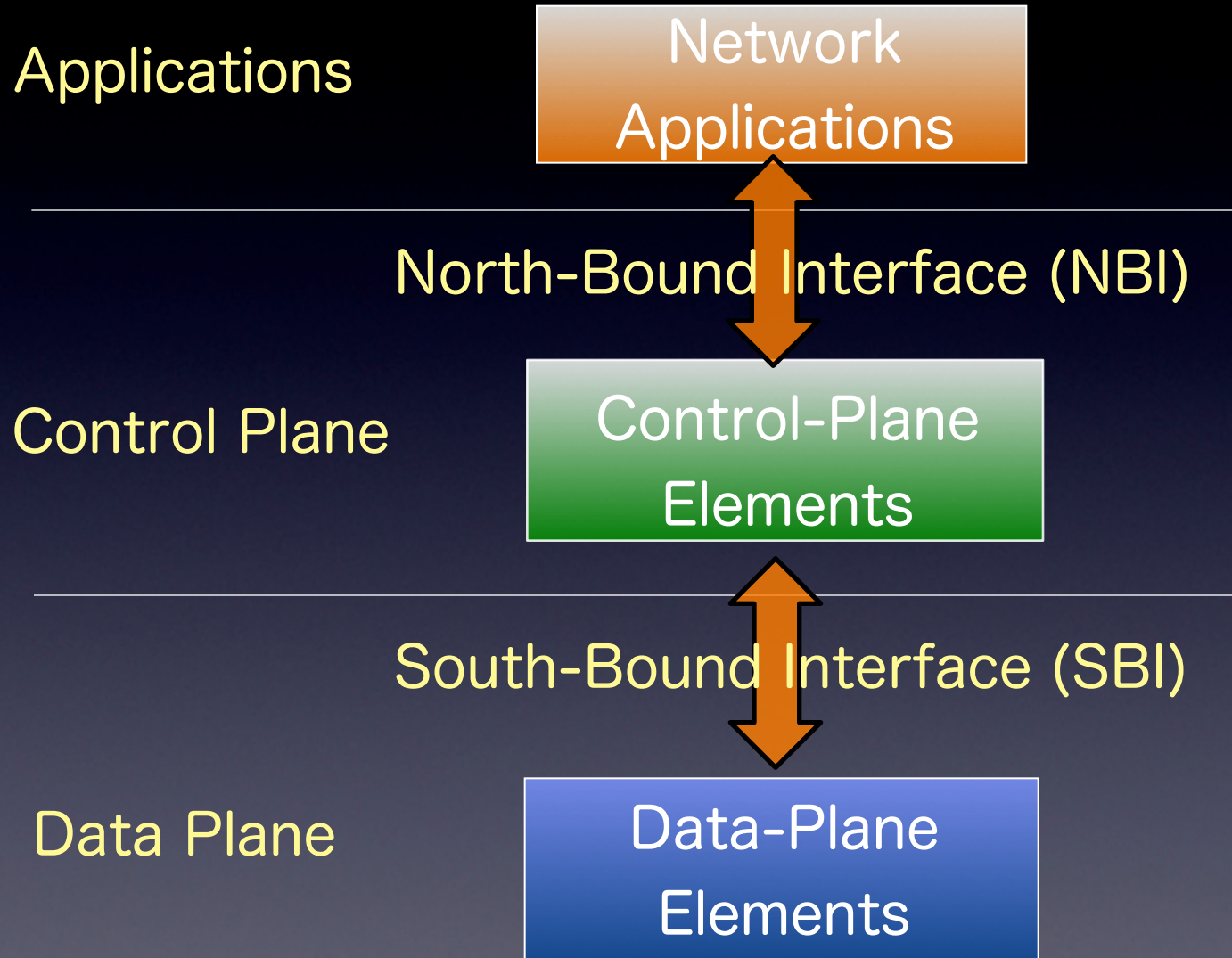
Aki Nakao

The University of Tokyo

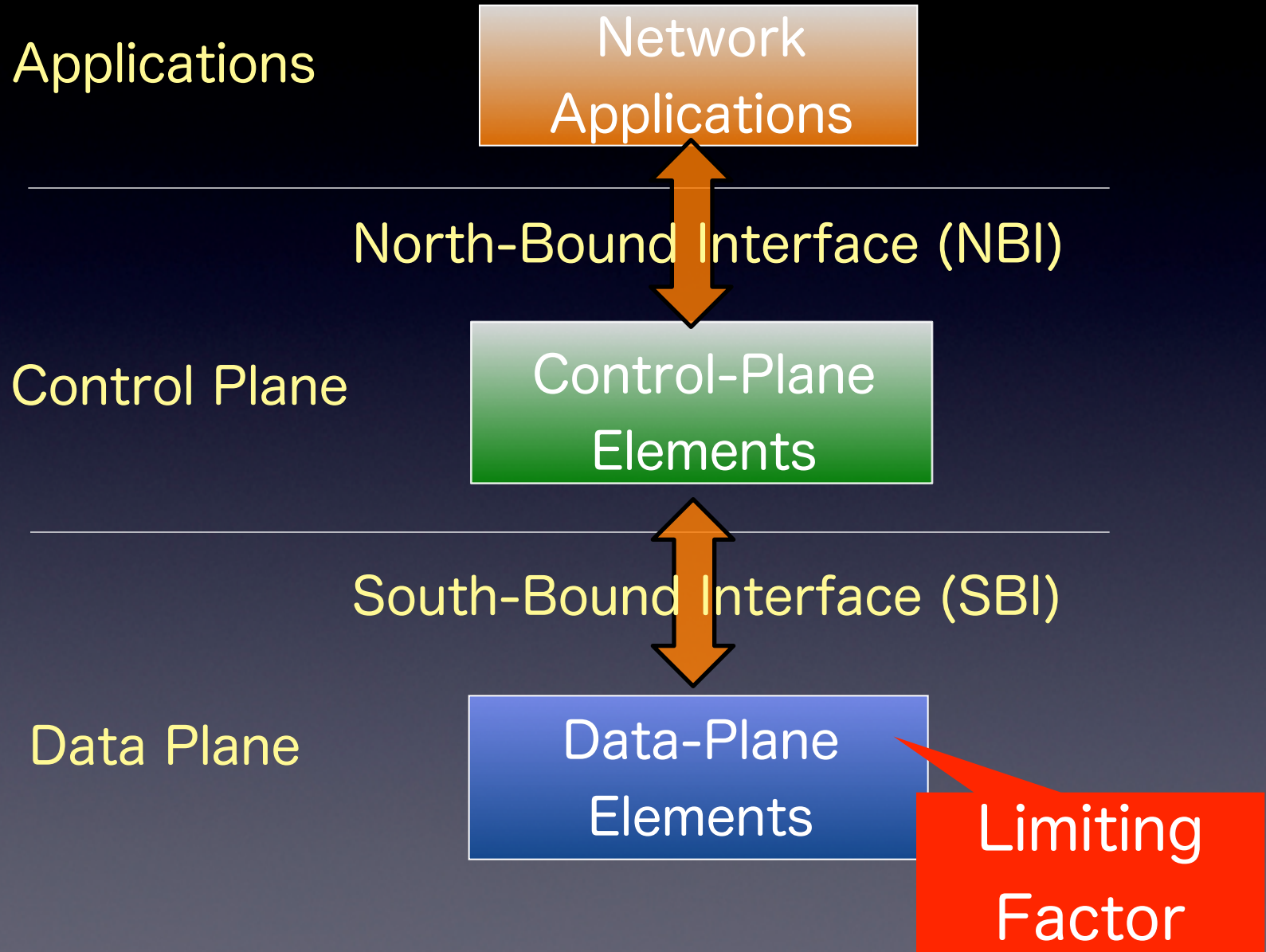
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2013/11/19

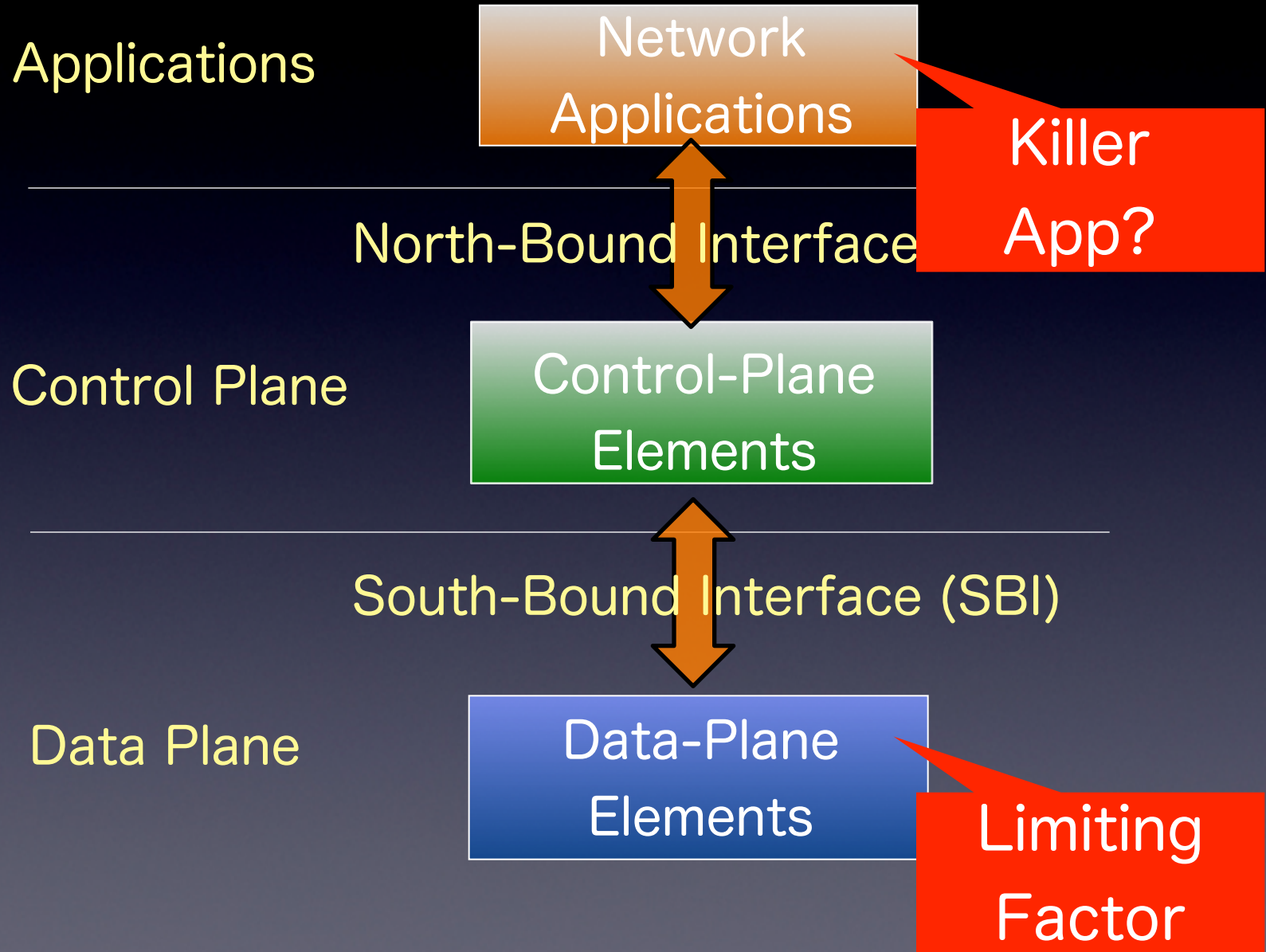
SDN Architecture



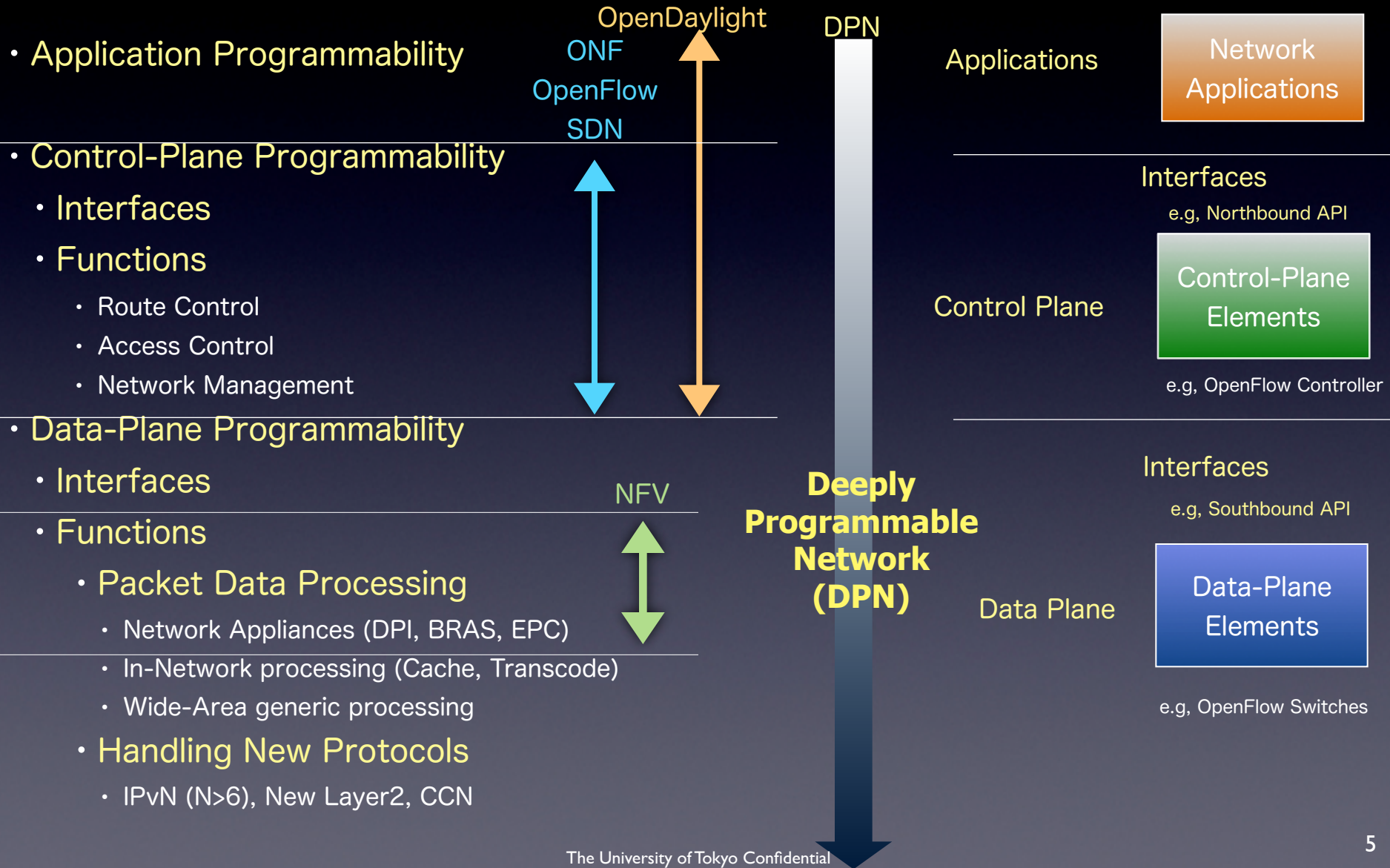
SDN Architecture



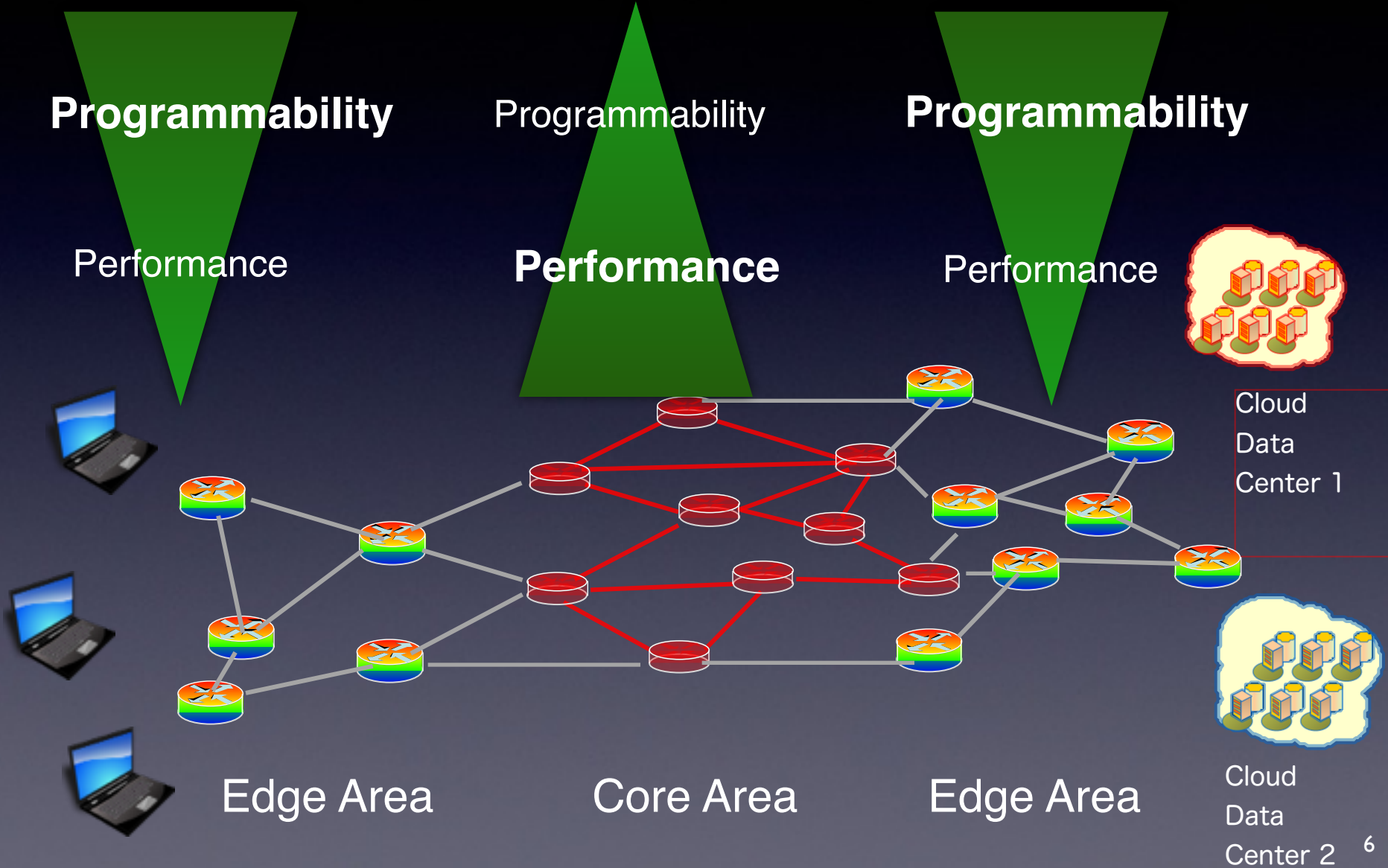
SDN Architecture



Deeply Programmable Network

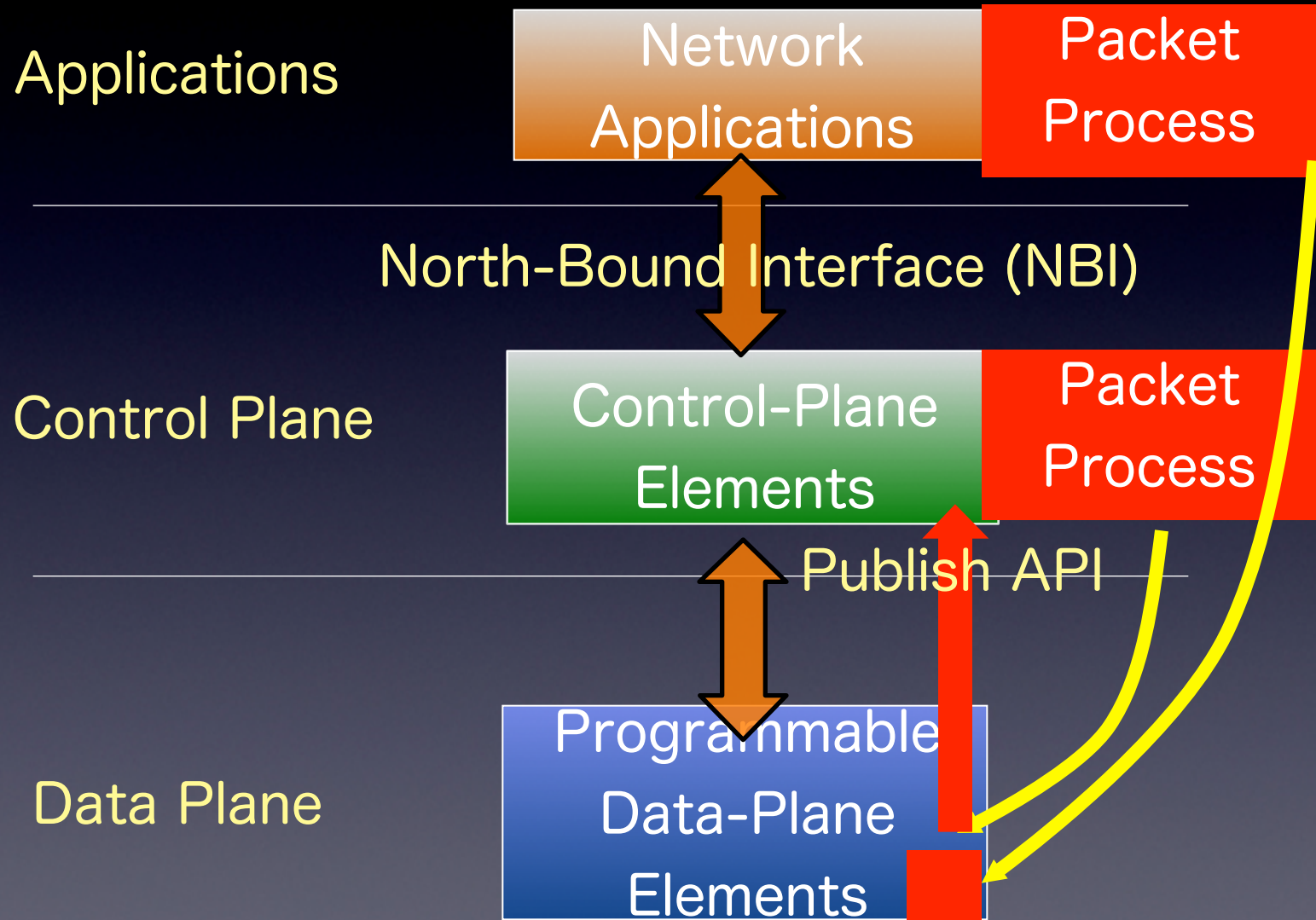


Programmability / Performance Tradeoff



Data-Plane Programmability

Extends Current SDN



Challenges

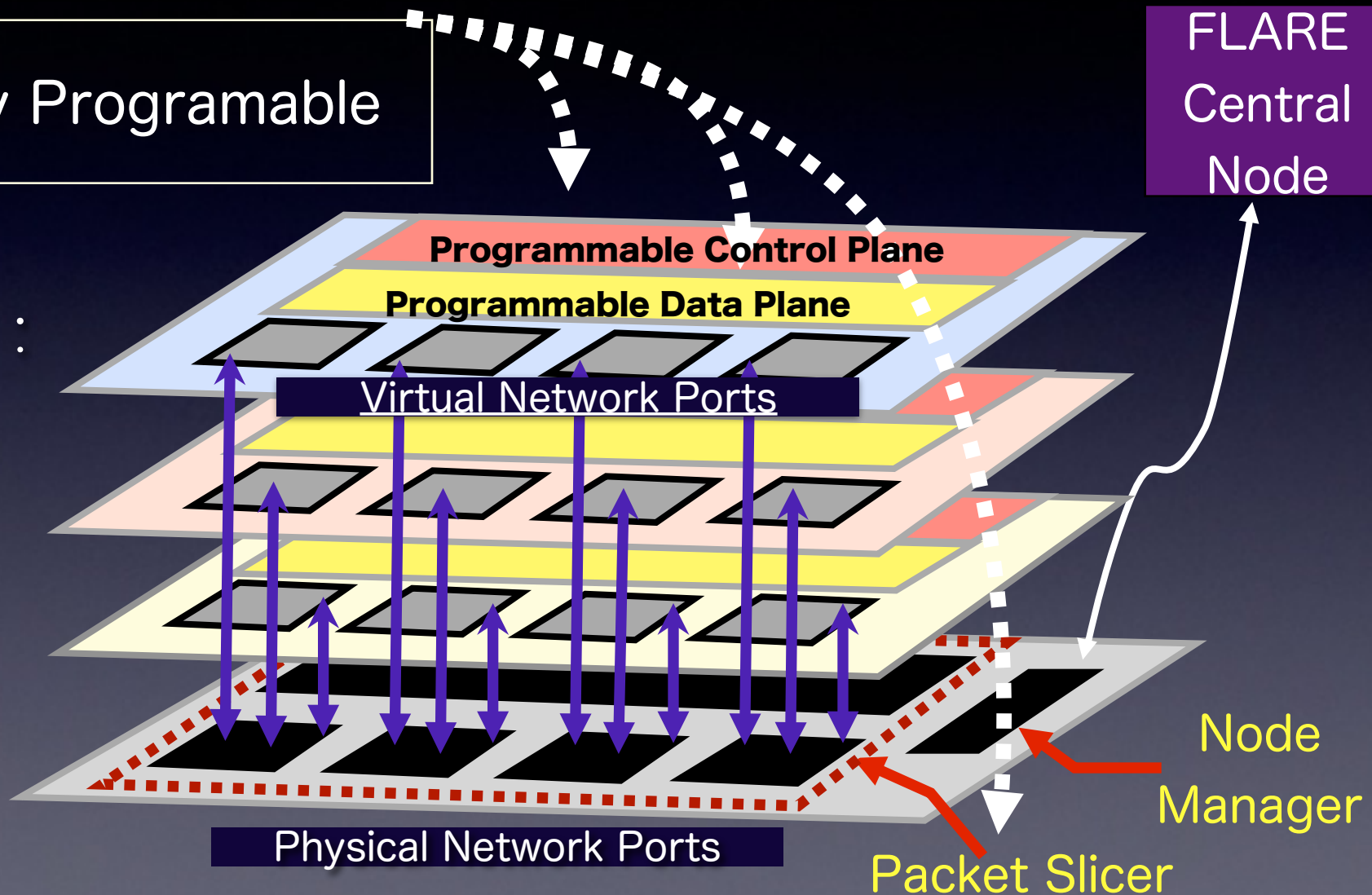
- Deep programmability
- (Reasonable) Performance
- Multiple Concurrent Logics

FLARE's Approach to these challenges

- Linux(OSS)+Toy-Block Data Plane Construction
- Many-Core Network Processor + General Purpose Processor
- Virtualization/Resource Container

FLARE Node Architecture

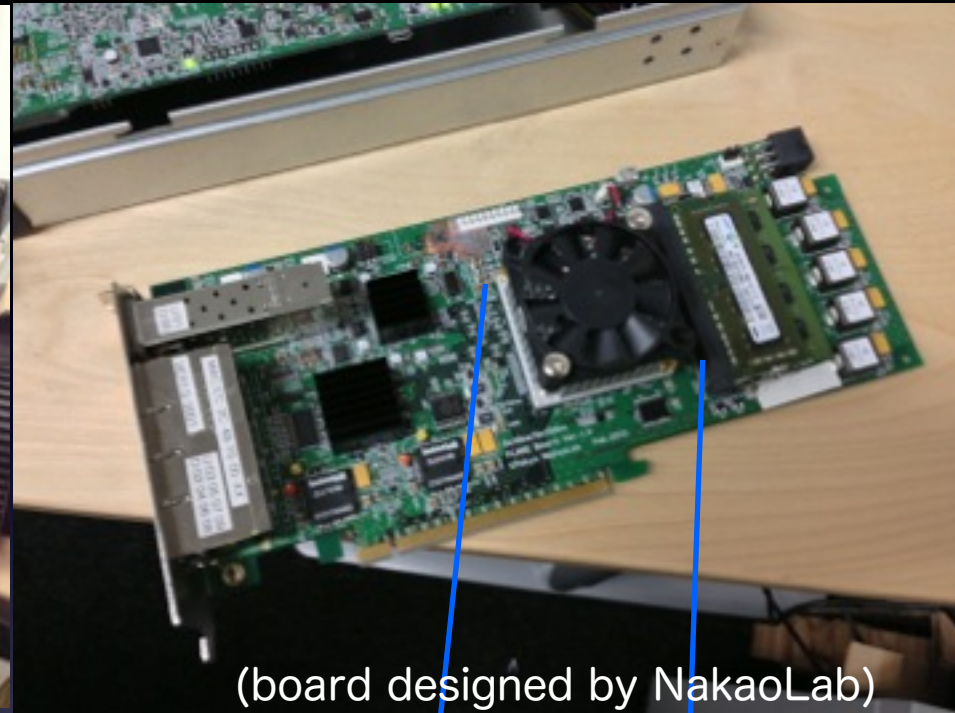
Fully Programmable



FLARE Node Implementation

x86
Processor

Many Core
Processor



(board designed by NakaoLab)

36-72 cores

(upto 100-200 cores in future)

Hierarchical Resource Management

- General Purpose Processor(s)
- Network Processor(s)
- ...and more types of processors

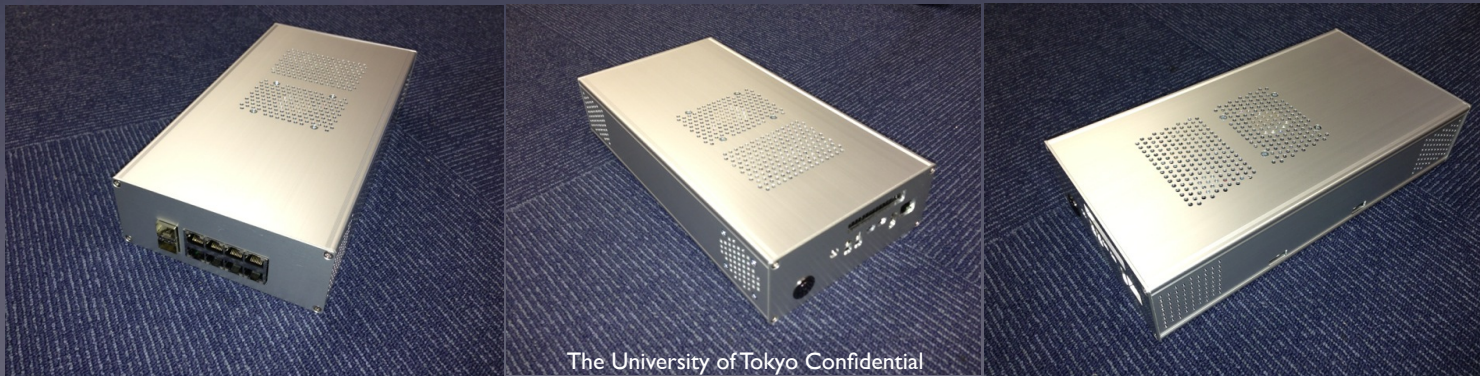


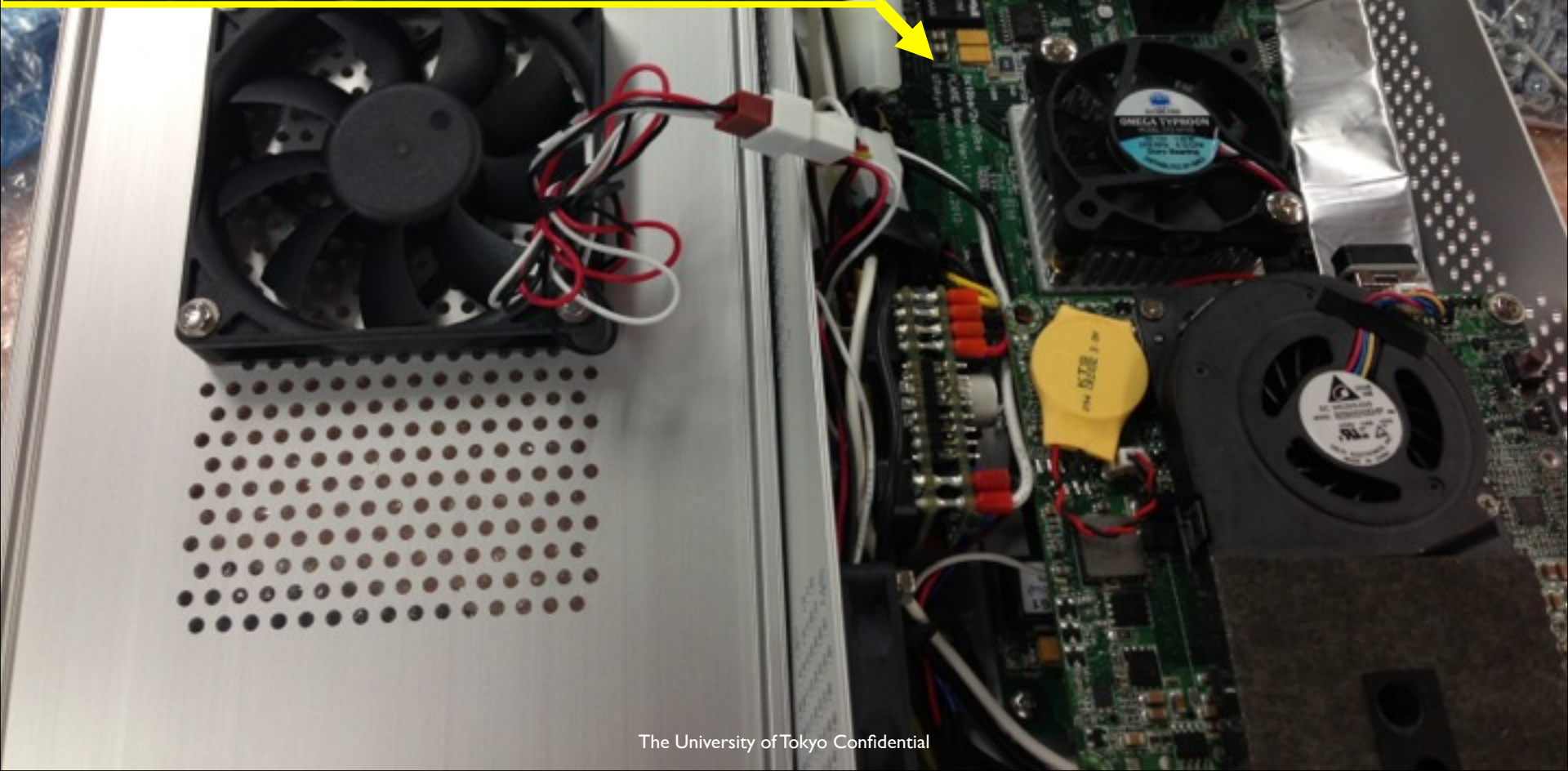
Roadmap of FLARE nodes



FLARE Mini now available...

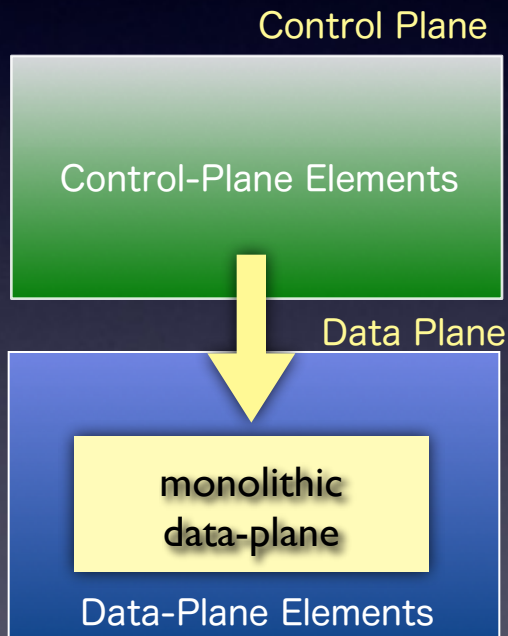
- Small Form Factor: 15cm x 6cm x 28cm
- Low power : 120W
- (Data Plane) Programmable node a graduate student can bring home and play with
- Capacity: 40G(current) ~ 80G (planned)
- Network I/F: 10Gx2 + 1Gx8 (current) 10Gx8(planned)
- Preinstalled with network function elements that can be combined to enable arbitrary network functions e.g., OpenFlow 1.0/1.3, Packet Generator, Pcap Replay





Data-Plane API and Toy Block Networking

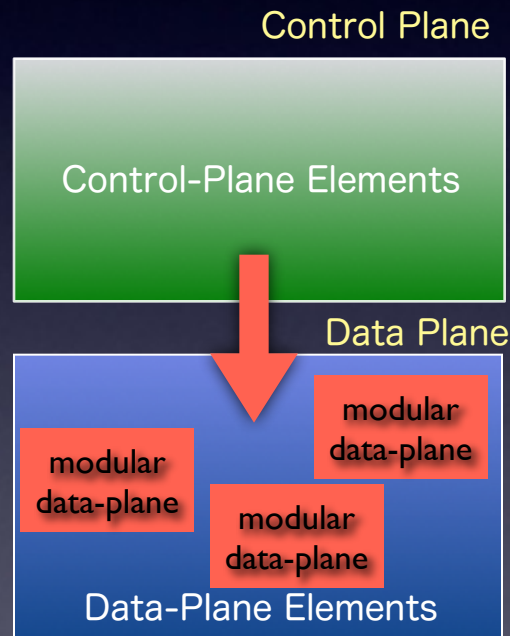
SDN-style API



e.g.,

openflow-style

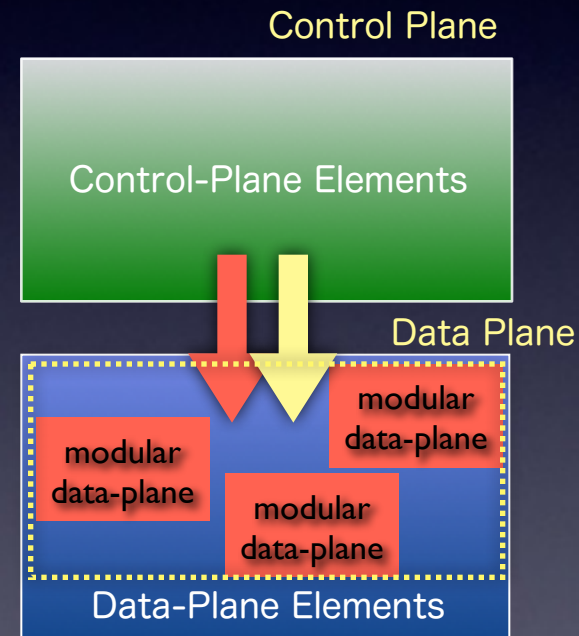
Hot Config Plug-in/out



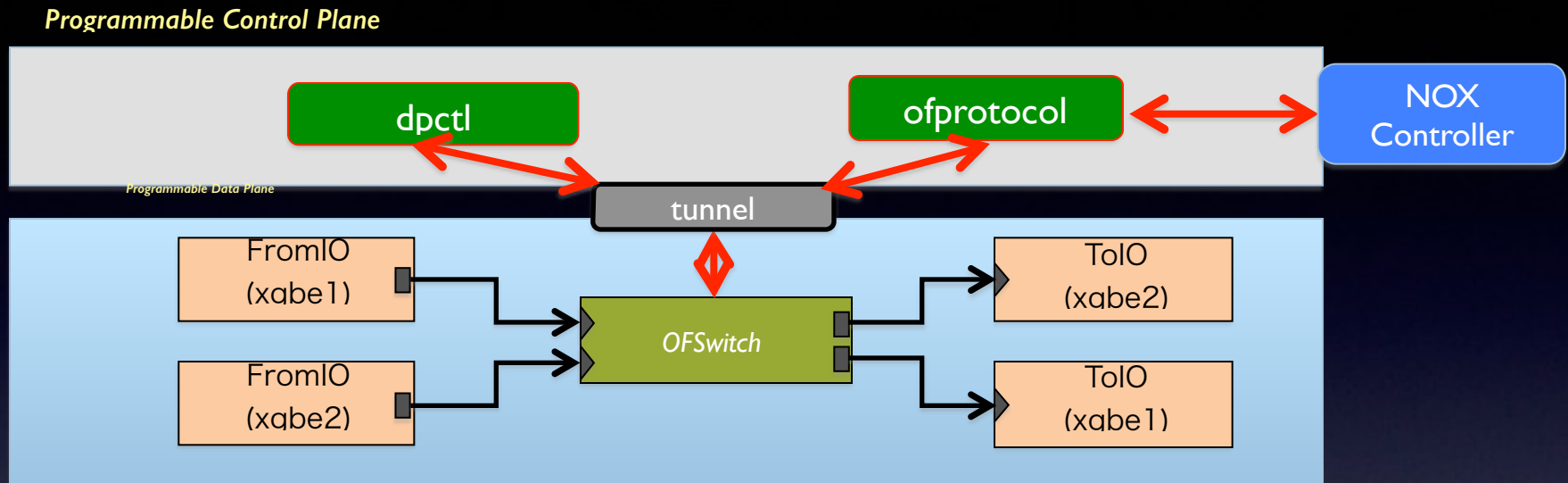
e.g.,

Object Oriented

Both API + Hot Config



FLARE Programming Model in Sliver



Multi-Threaded Modular Programming
e.g., Click Software Modular Router (multi-threaded)

- Arbitrary switch logic(s) can be implemented

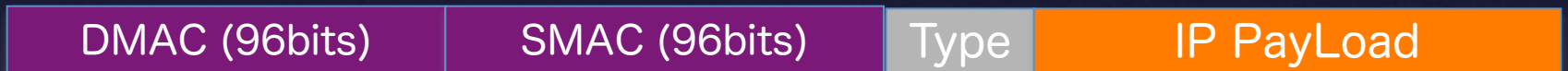
L2 Programmability

Extended (96bit) MAC switching

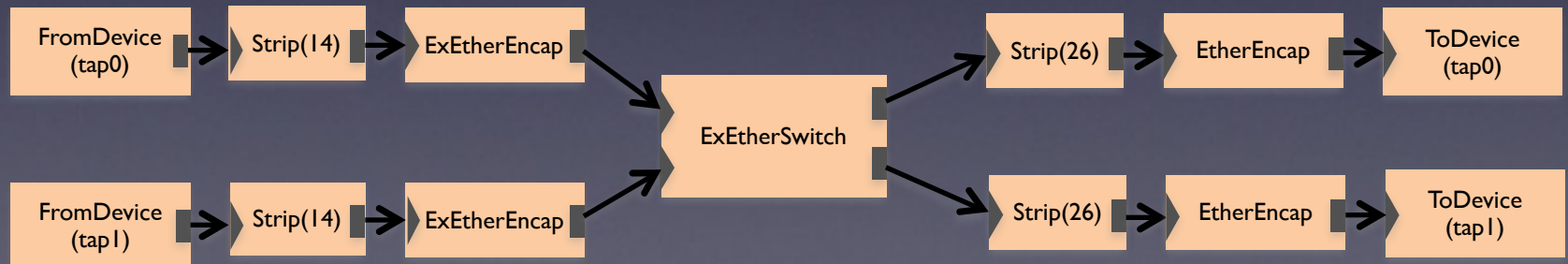
Traditional Ethernet Frame:



Extended Ethernet Frame with Extended MAC:

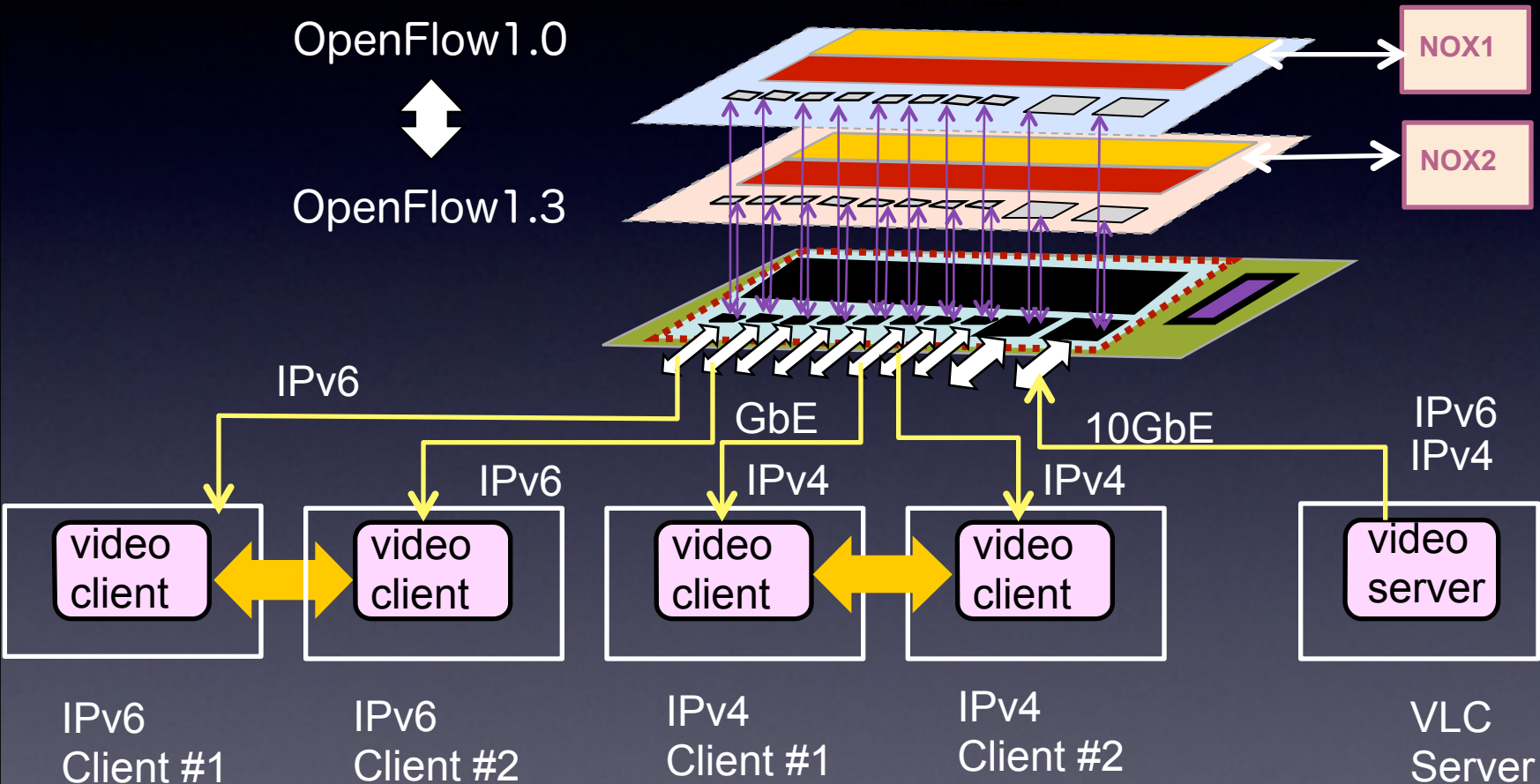


Prototype with Click



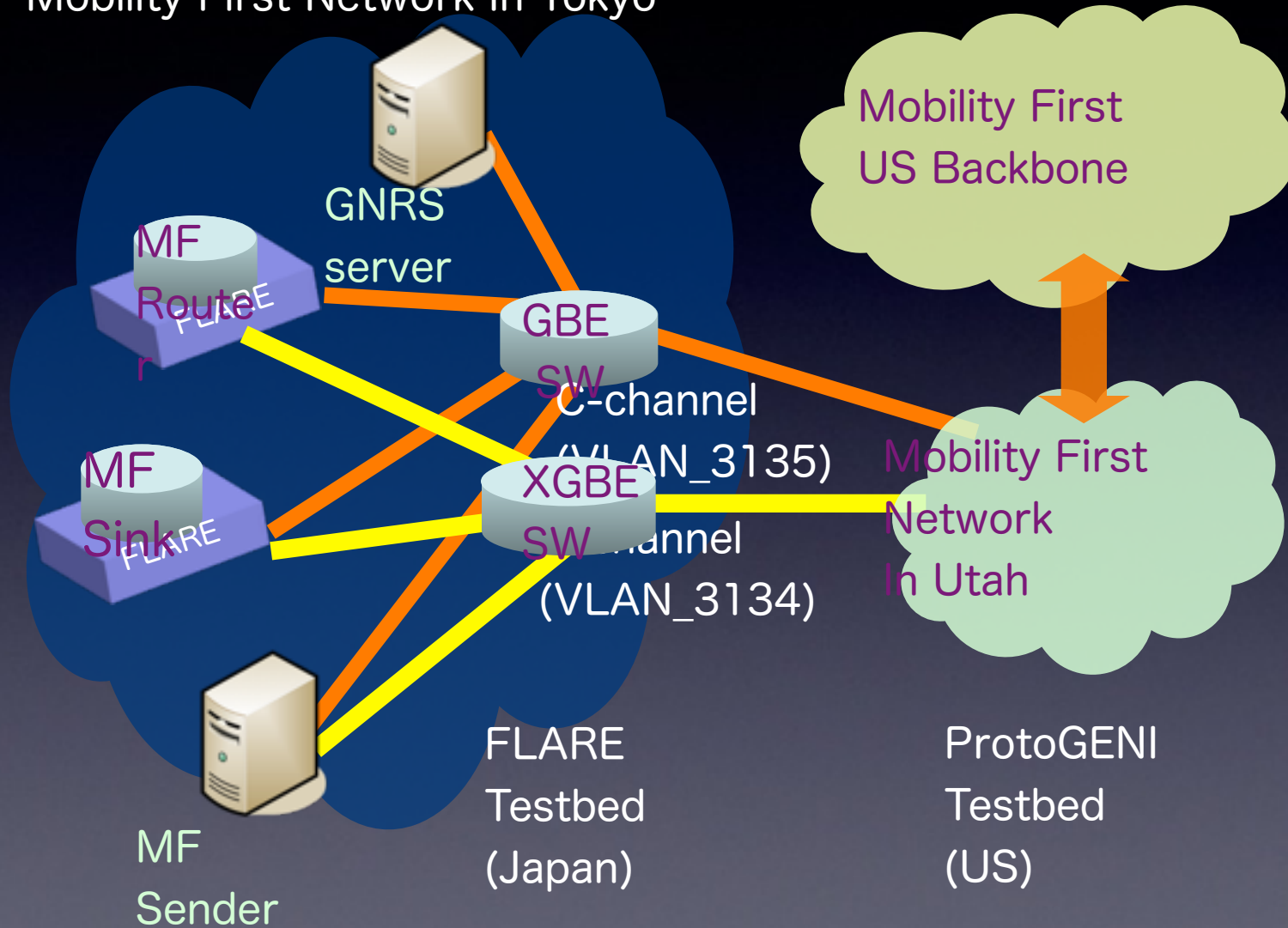
Multiple SDN Logics

(OpenFlow 1.3 and OpenFlow 1.0)



PaF, PiF, PoF, Non-IP Protocol

Mobility First Network In Tokyo



Window-based Arbitrary Bit Matching

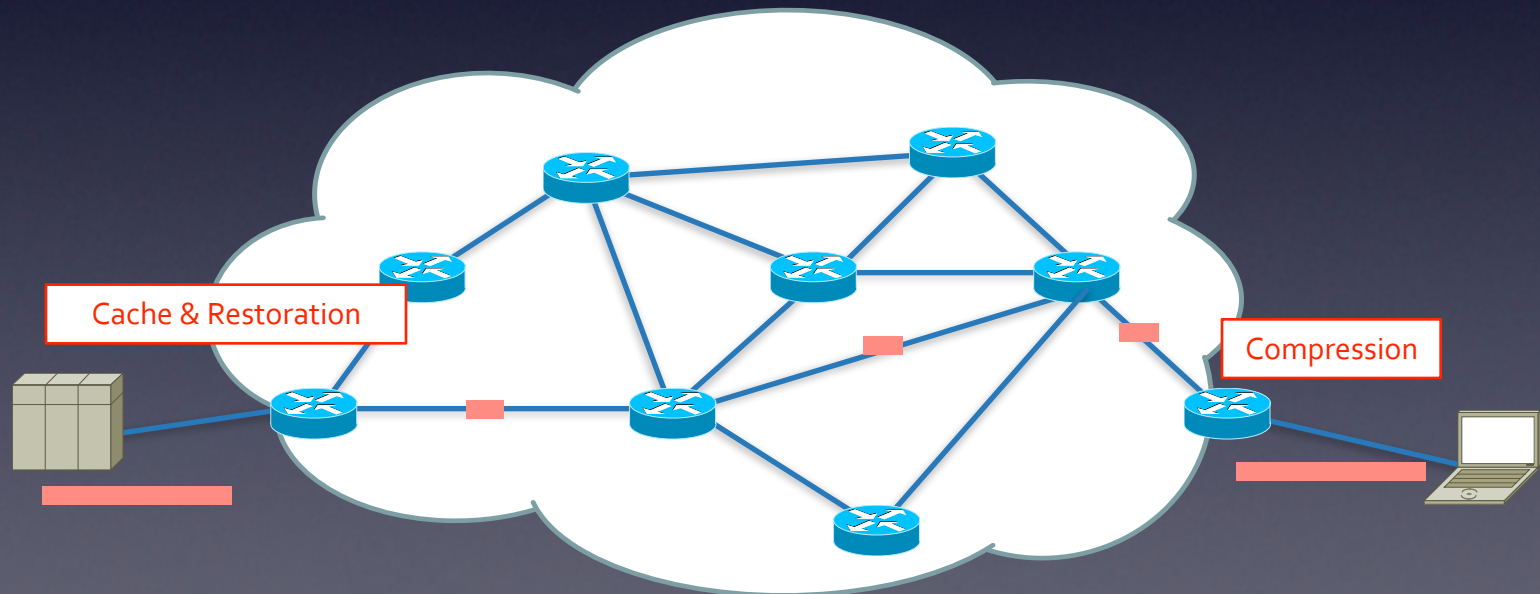
Arbitrary bit matching as in openflow pattern matcher is costly due to expensive memory operation per packet



Set a window to minimize per-packet memory operations
Improve performance while keeping flexibility

YouTube Packet Cache

- Reduce cross-ISP redundant traffic
- Matching L7 (URL) not headers!



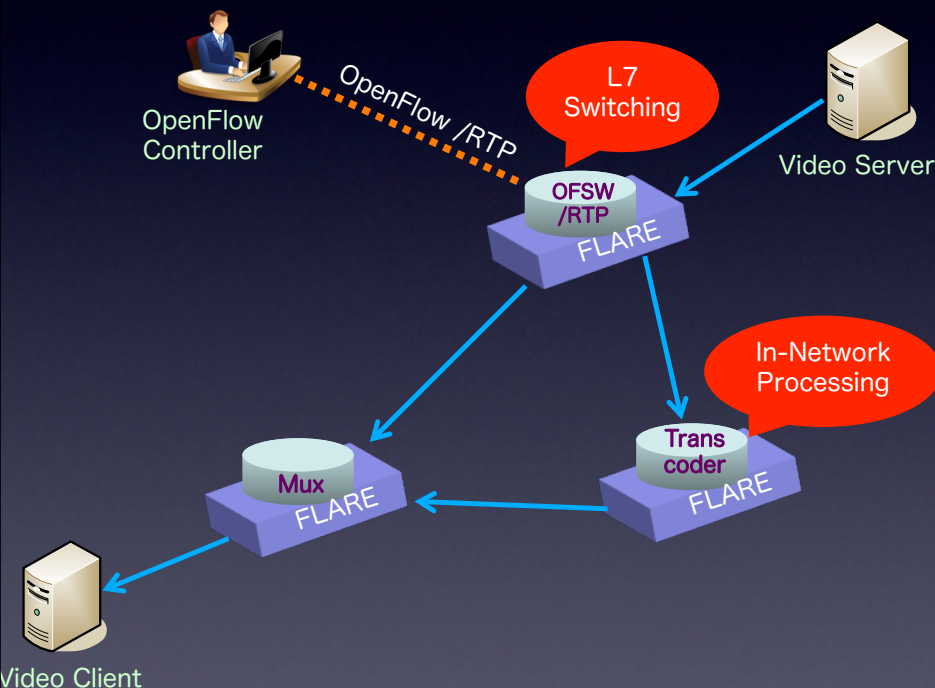
L7 Switching and In-Network Processing

L7 Switching

FLARE supports deeply programmable SDN solutions such as **arbitrary-bits and arbitrary offset matching** and **definition of proprietary APIs** achieving both flexibility and performance

In-Network Processing

Video transcoding can be preformed in real time on either D-plane (many-cores processor) or C-plane (Intel-CPU).



Conclusion

- **Deep Programmability** refers to the extensive programmability including Control-plane, Data-plane (including non-IP handling), (re)defining APIs in SDN, etc.
- **Deeply Programmable Network** research encourages “clean-slate” thinking and redesigning the network and lifts the limitation in traditional networking and even in the current SDN.