Implementation of the hardwired AFDX NIC

Pusik Park

parksik@keti.kr

SoC Platform Research Center

Korea Electronics Technology Institute

KETI 전자부품연구원
Korea Electronics Technology Institute

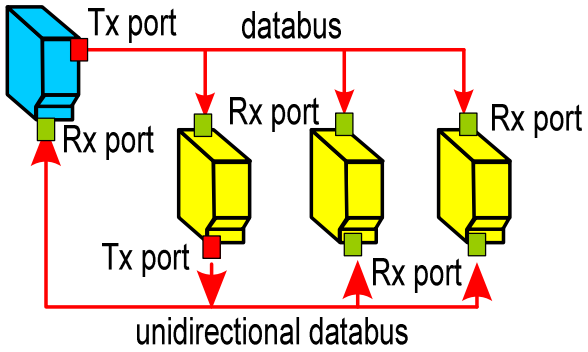
Agenda

- Overview of AFDX
- Conventional products
- Design issues
- Implementation
- Result
- Summary
- Q & A

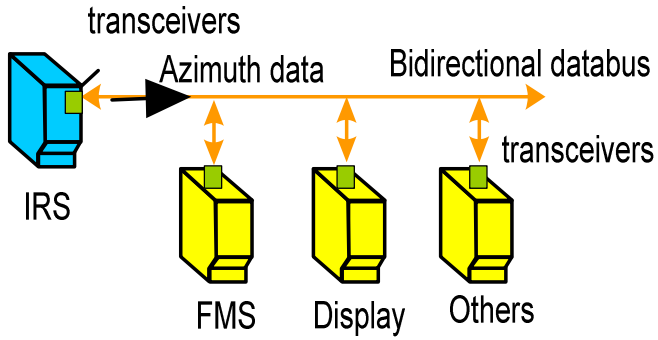
Aircraft Data Network (AND)

- Control Network
  - Real-time communication among sensors, actuators, and LRUs
  - Wired-network
- Crew Network
  - Wireless network between a crew and an infrastructure
- Passenger Network
  - LAN for infotainment in a cabin
  - Internet

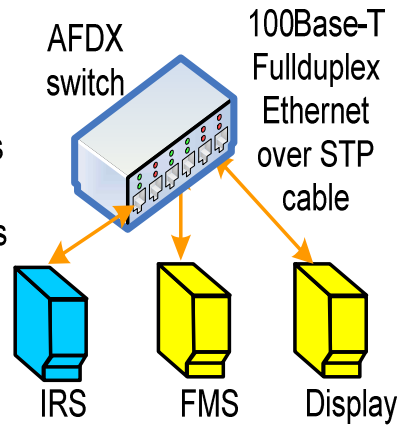
Avionics Network



(a) Unidirectinal bus방식 (ARINC 429)

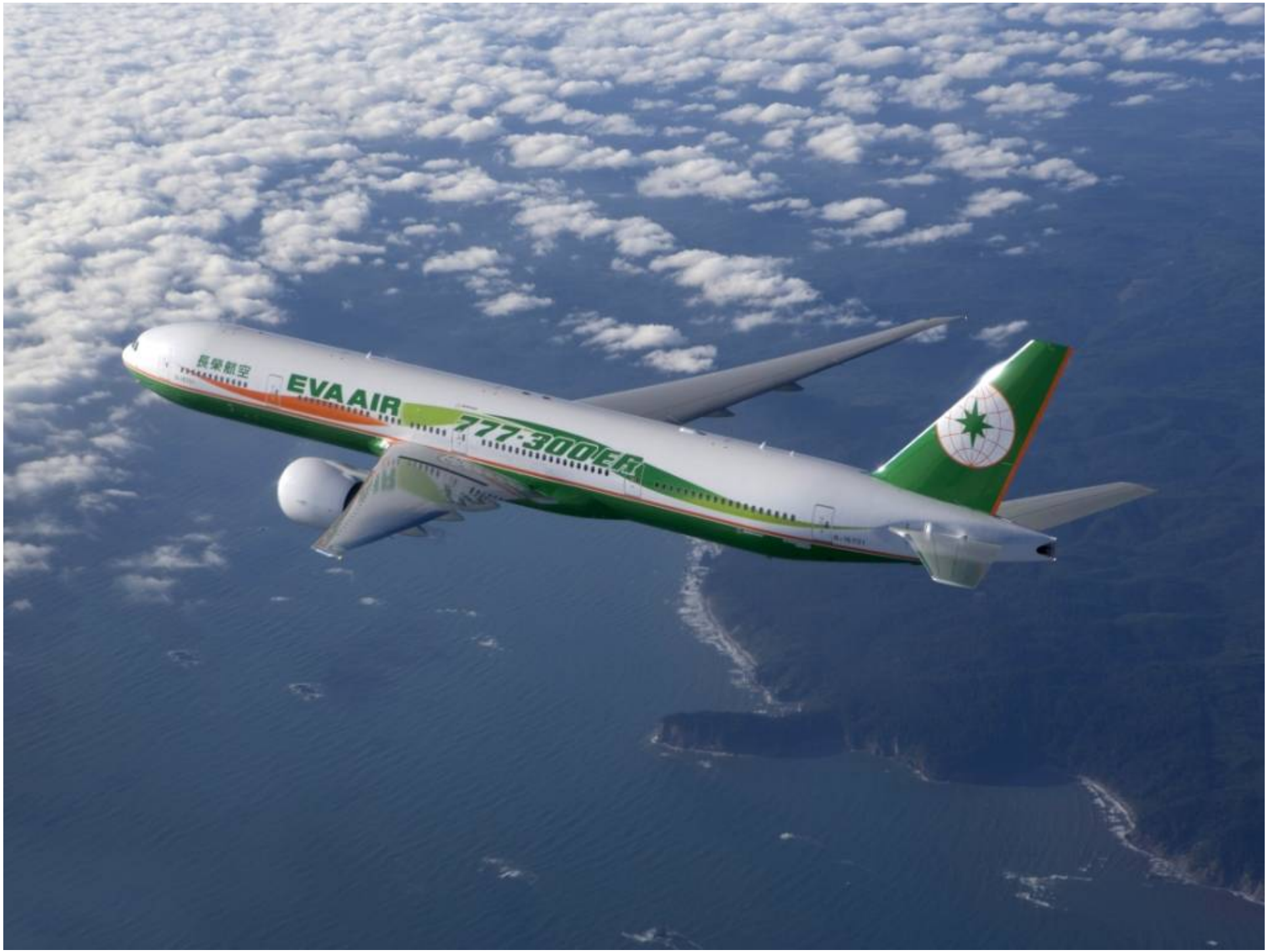


(b) bidirectional bus방식 (ARINC 622/ MIL-STD-1553)



(c) Fullduplex Ethernet Switch방식 (ARINC664)


Astraeus


長榮航空
EVA AIR
777-300ER


KOREAN AIR

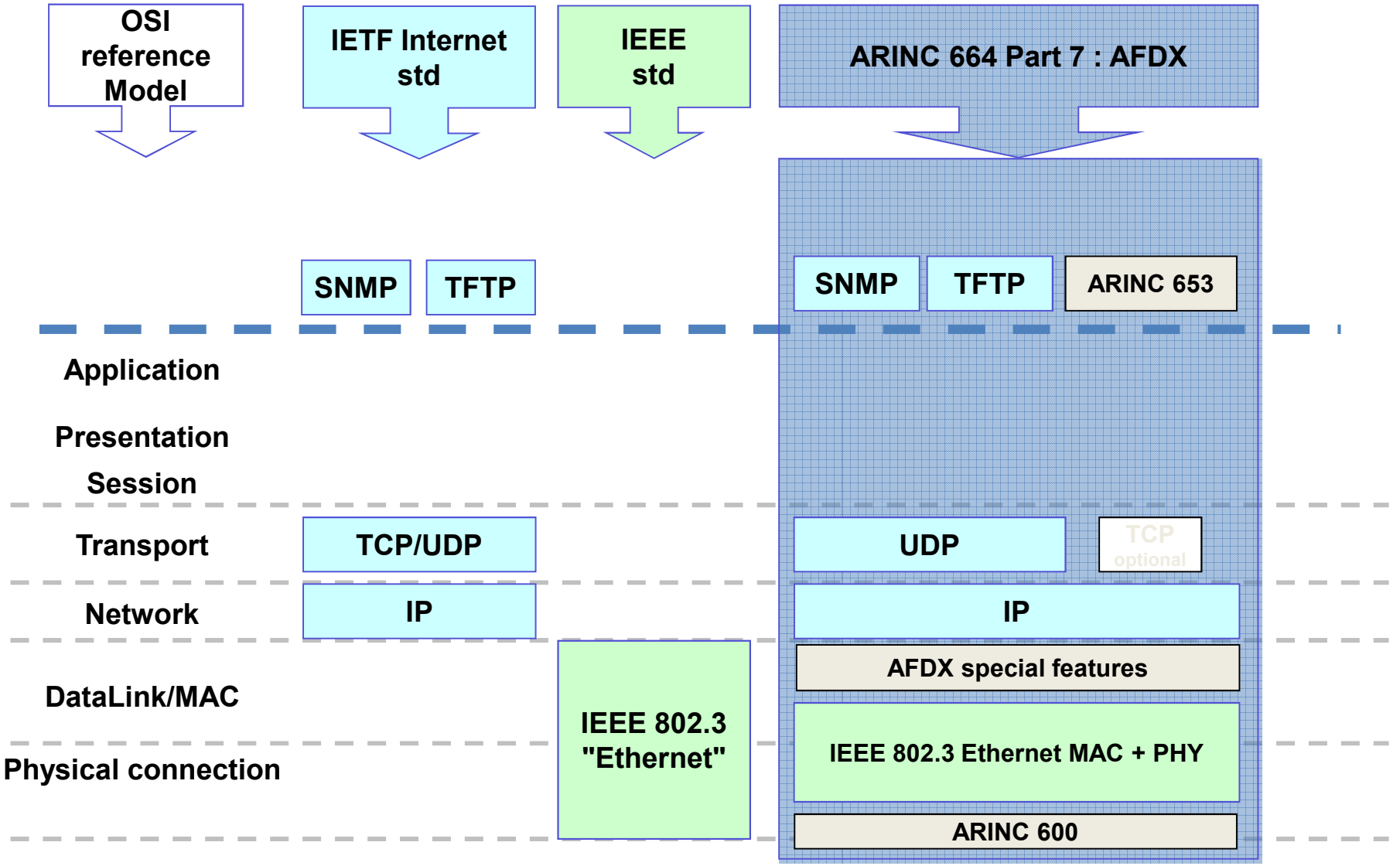
KETI 전자부품연구원
Korea Electronics Technology Institute

AFDX Overview

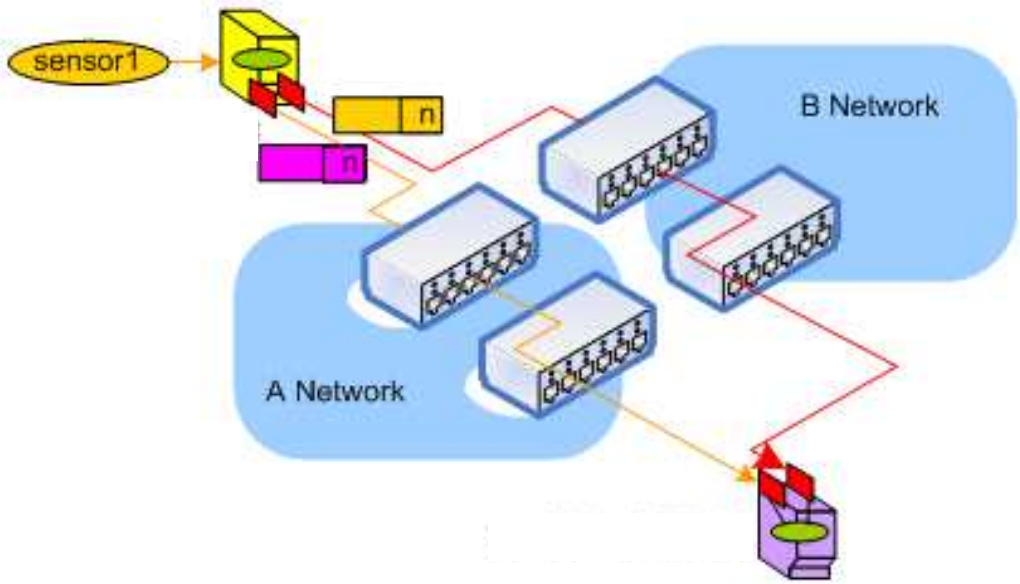
- Avionics Full Duplex Switched Ethernet
- Publish
  - ARINC 664 Part 7
- Requirement
  - Time constraint
  - Safety
- COTS
  - IEEE 802.3 Ethernet technology for physical layer
  - Internet for upper protocol layer

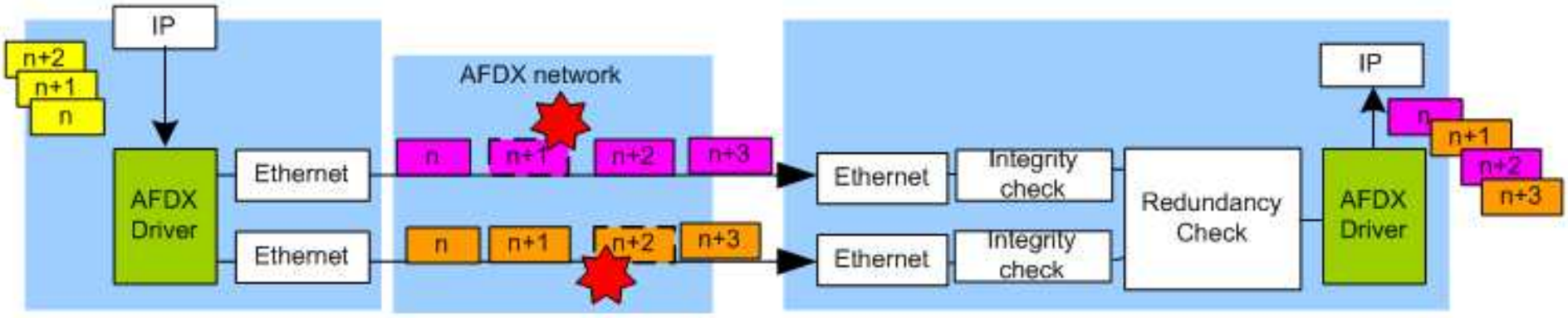
- Features
  - Standardization
  - Real-time
  - Low cost
  - Compatibility
  - Light-weight
  - Redundancy

AFDX Standard



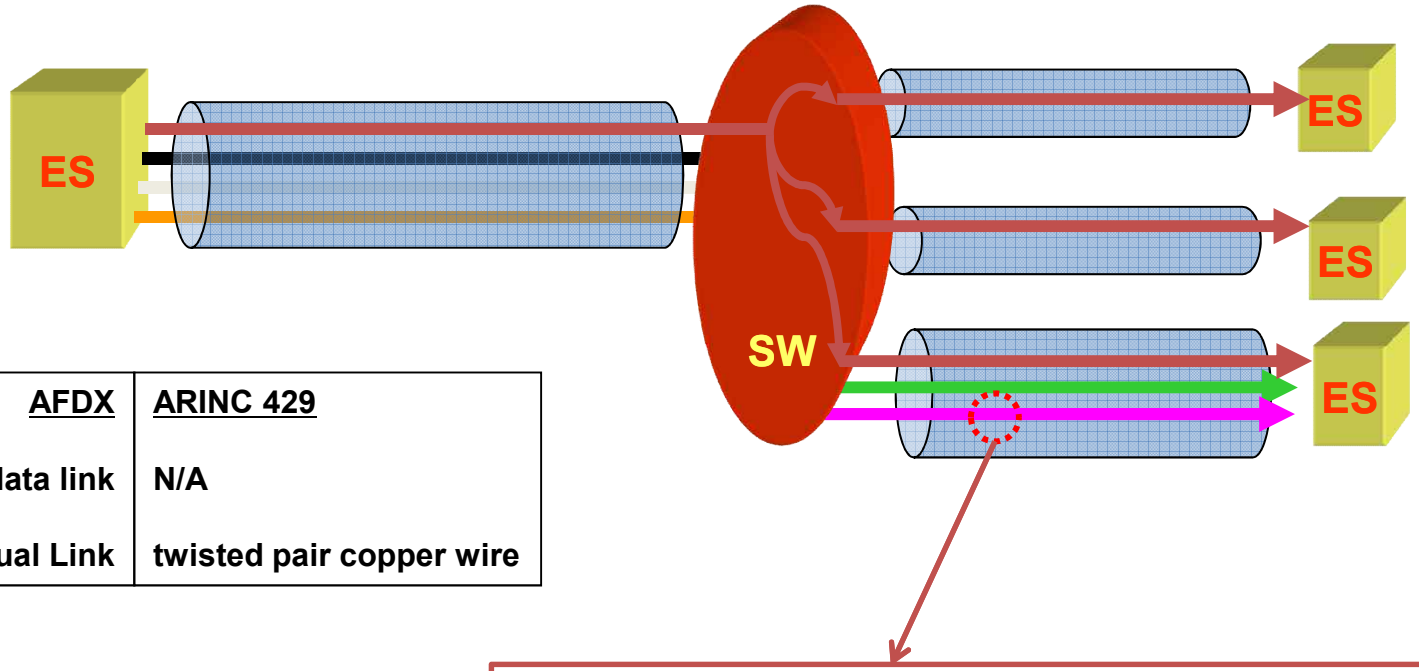
AFDX Technology





AFDX Technology

- Virtual Link (VL)

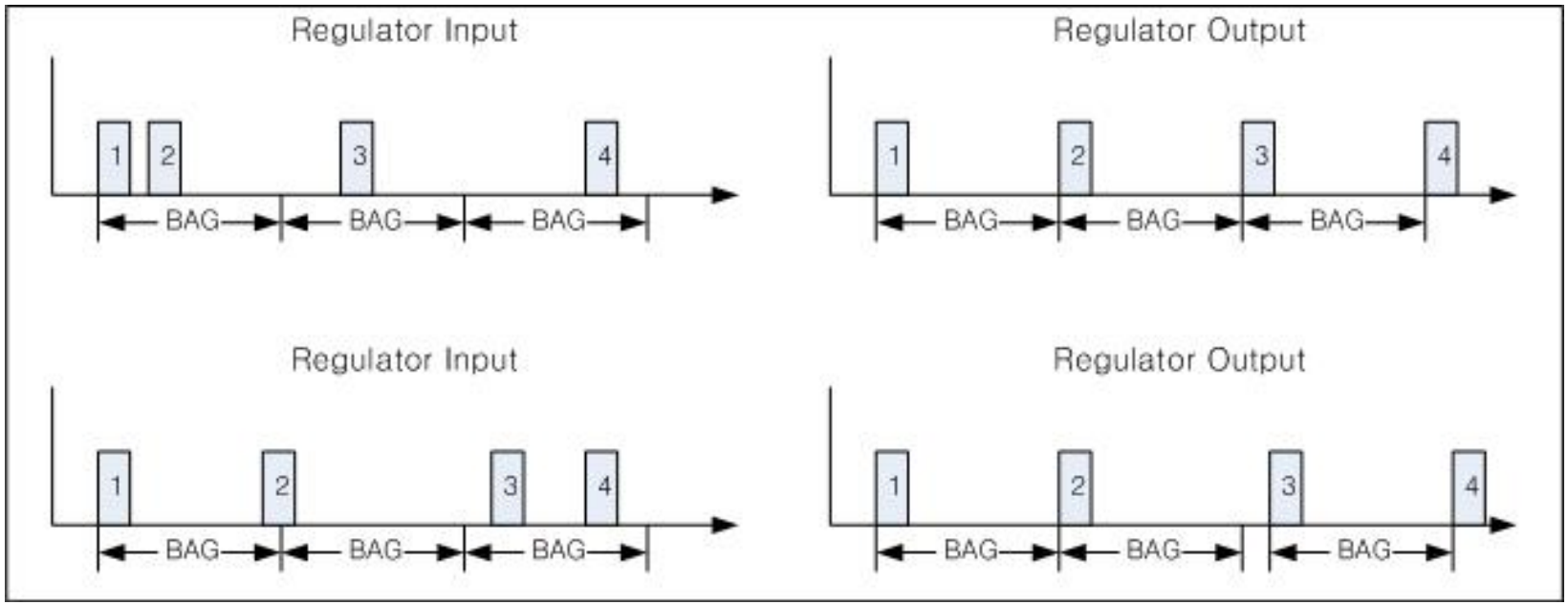


AFDX	ARINC 429
Ethernet data link	N/A
Virtual Link	twisted pair copper wire

Compatible with a channel of the ARINC 429

AFDX Technology

- Bandwidth Allocation Gap (BAG)

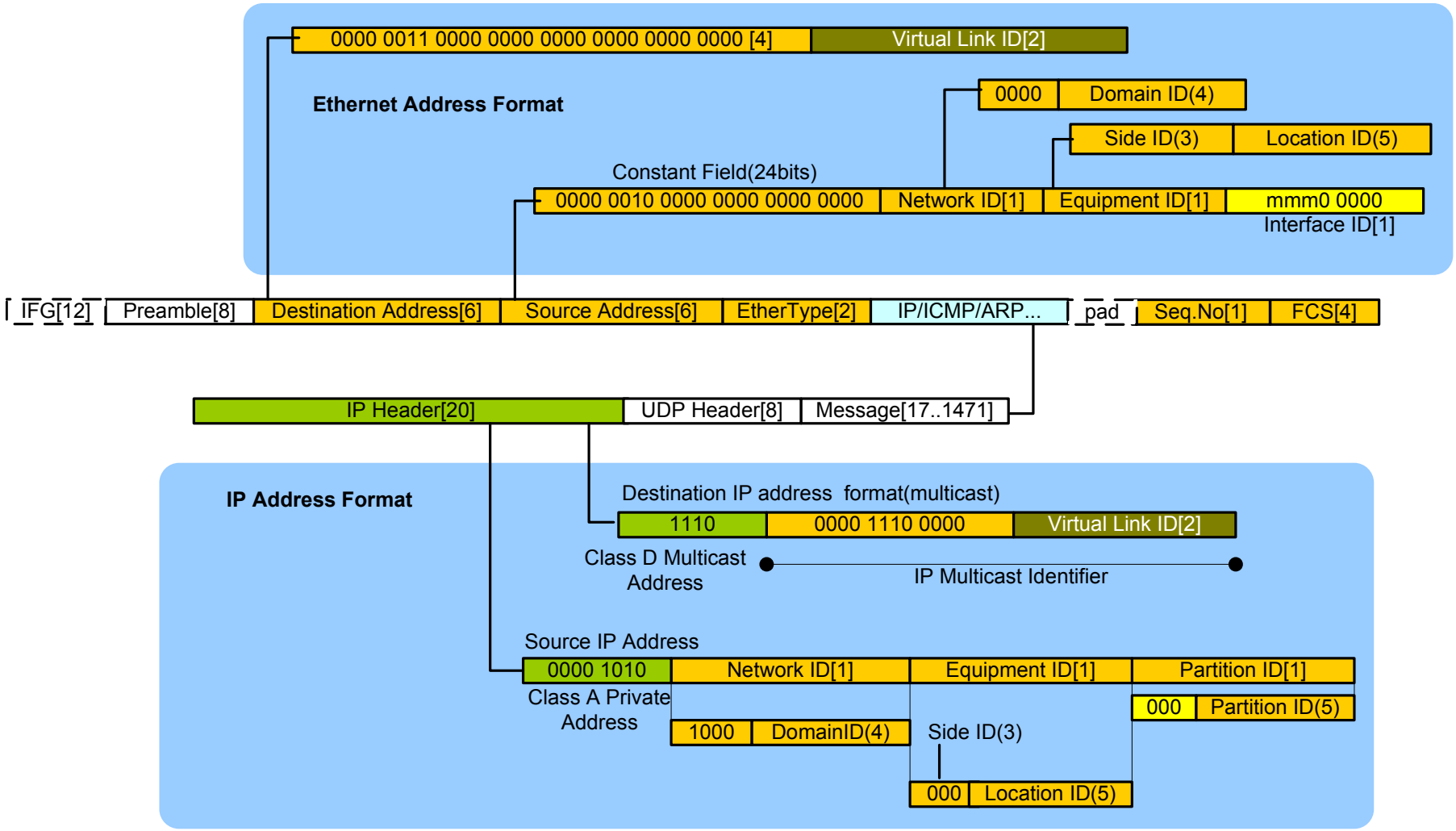


AFDX Technology

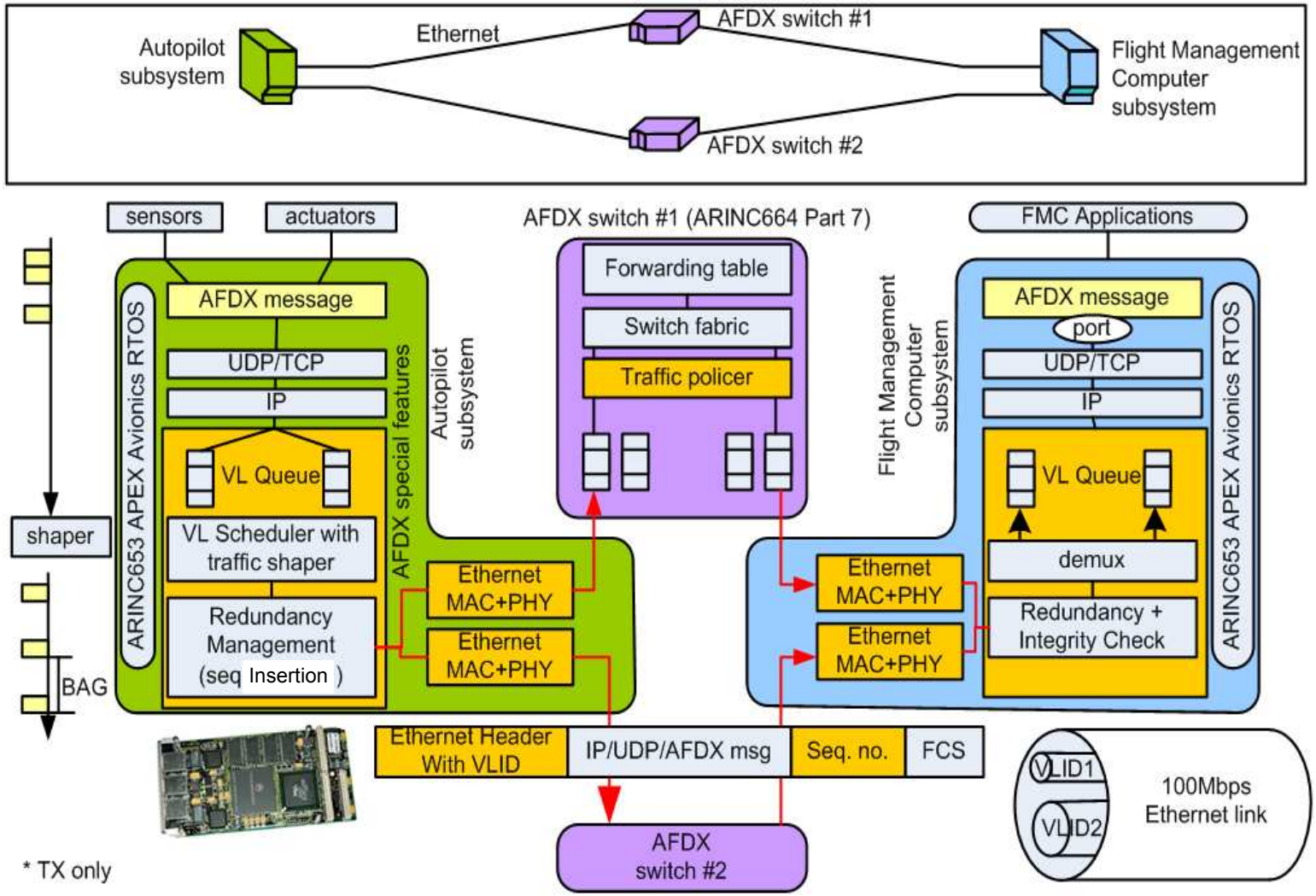
- Bandwidth Allocation Gap (BAG)
  - The minimum interval between adjacent frames on a virtual link
  - 1 ~ 128 [ms]
- Lmax
  - The maximum frame length on a virtual link

$$\text{Bandwidth(bps)} = \frac{L_{\max}(byte)\times 8}{BAG(milisecond)}\times 1000$$

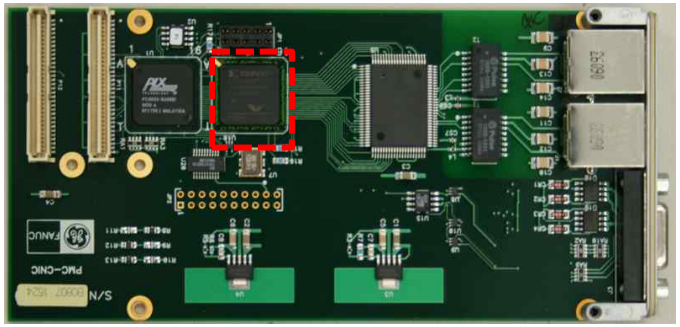
Frame Format

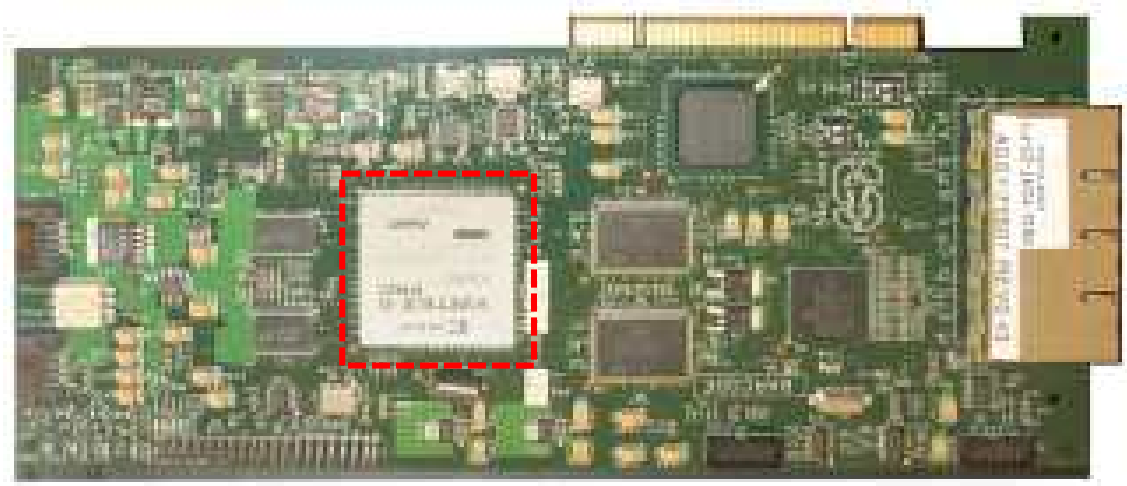


AFDX System


Autopilot subsystem
Ethernet
AFDX switch #1
AFDX switch #2
Flight Management Computer subsystem
sensors
actuators
AFDX switch #1 (ARINC664 Part 7)
FMC Applications
AFDX message
UDP/TCP
IP
VL Queue
VL Scheduler with traffic shaper
Redundancy Management (seq Insertion)
ARINC653 APEX Avionics RTOS
AFDX special features
Autopilot subsystem
Ethernet MAC+PHY
Ethernet MAC+PHY
Forwarding table
Switch fabric
Traffic policer
Flight Management Computer subsystem
Ethernet MAC+PHY
Ethernet MAC+PHY
AFDX message
port
UDP/TCP
IP
VL Queue
demux
Redundancy + Integrity Check
ARINC653 APEX Avionics RTOS
shaper
BAG
Ethernet Header With VLID
IP/UDP/AFDX msg
Seq. no.
FCS
AFDX switch #2
VLID1
VLID2
100Mbps Ethernet link
* TX only

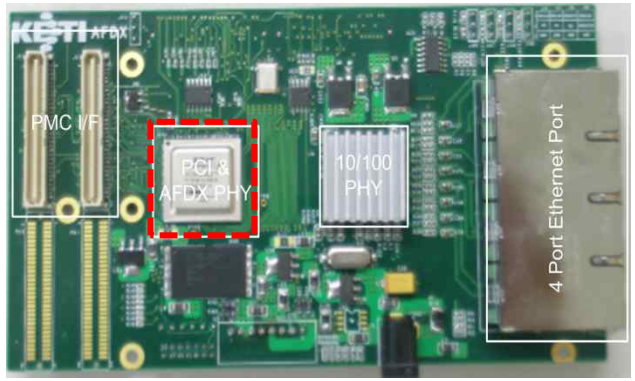
AFDX NIC Borad





Xilinx XC2VP50-7FF1152

LUT 14,960/47,232 (31%)
RAMB16 106/232 (45%)

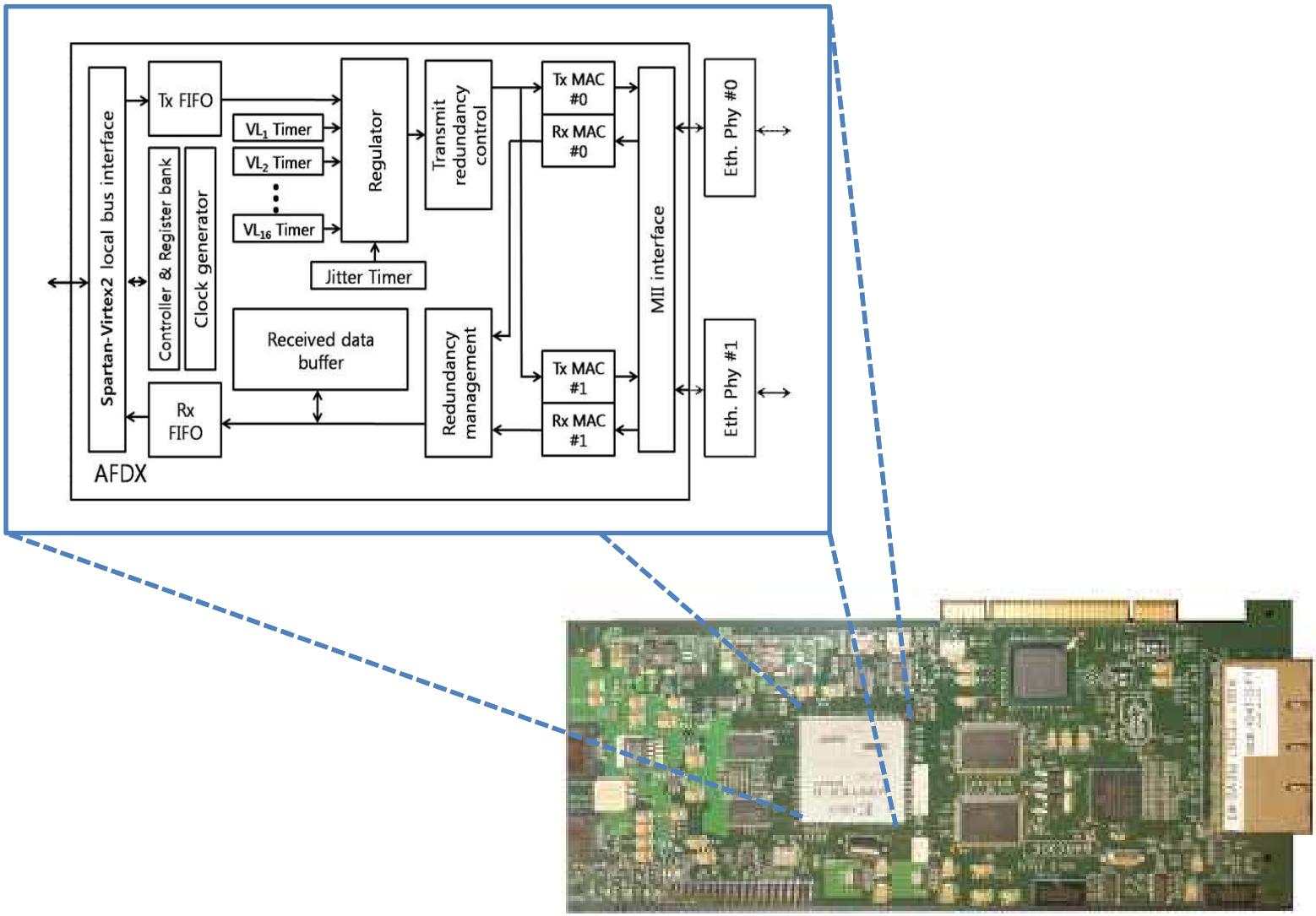


Xilinx XCV5LX50-3FF324

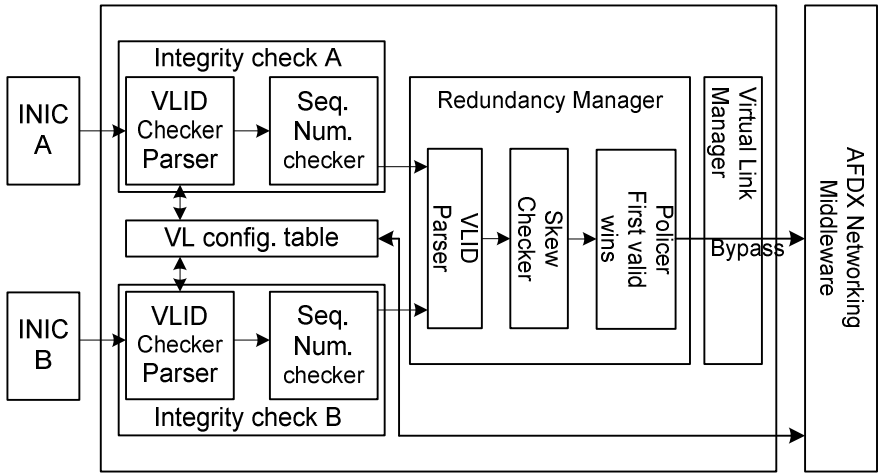
LUT 21,431/28,800 (74%)
BlockRam 44/48 (91%)

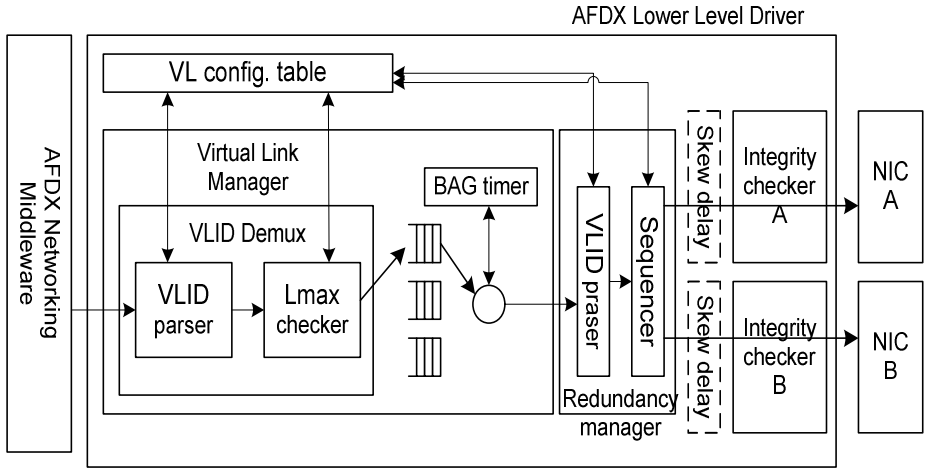
KETI 전자부품연구원
Korea Electronics Technology Institute

SW-based AFDX HW block diagram

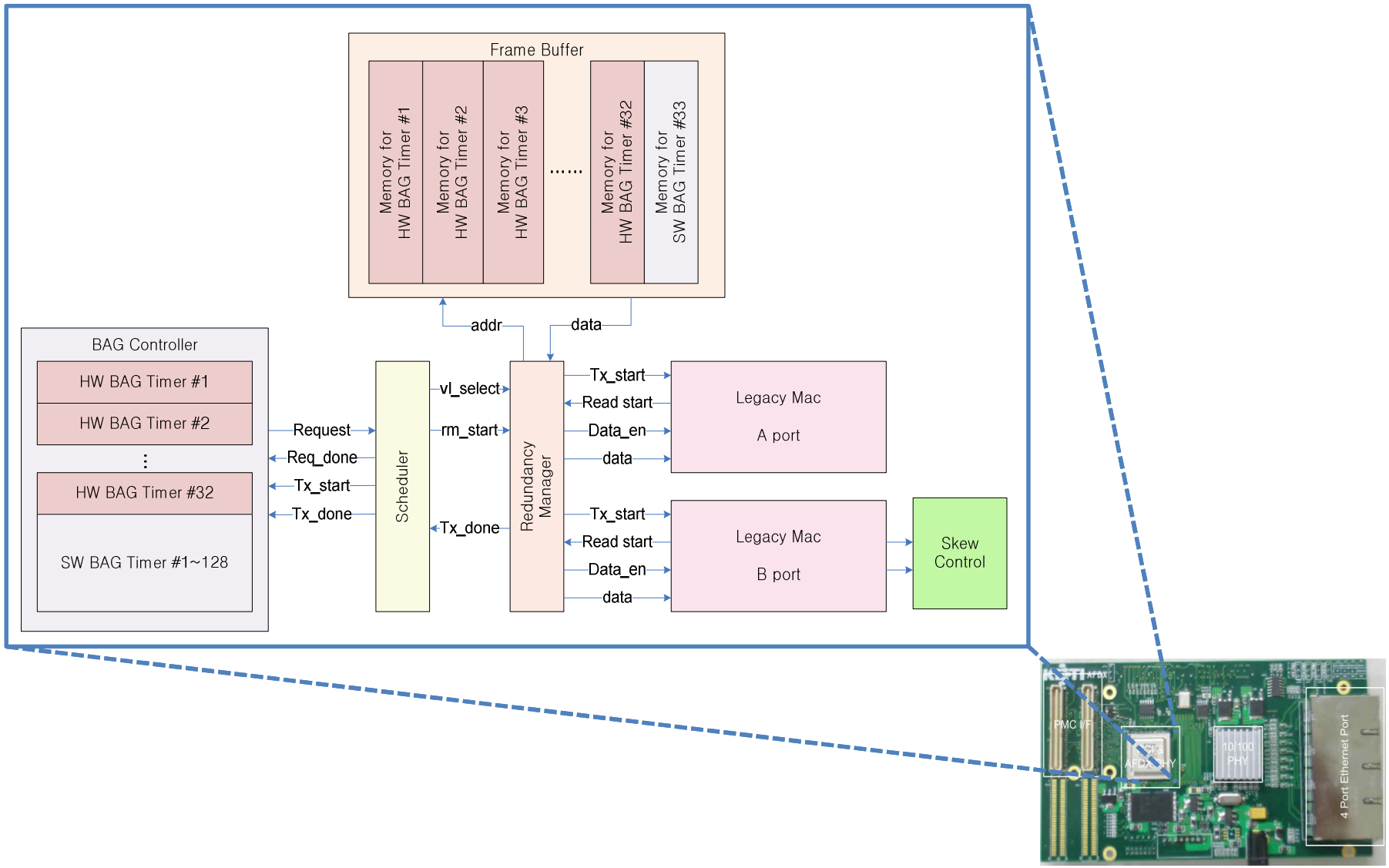


SW-based AFDX SW block diagram

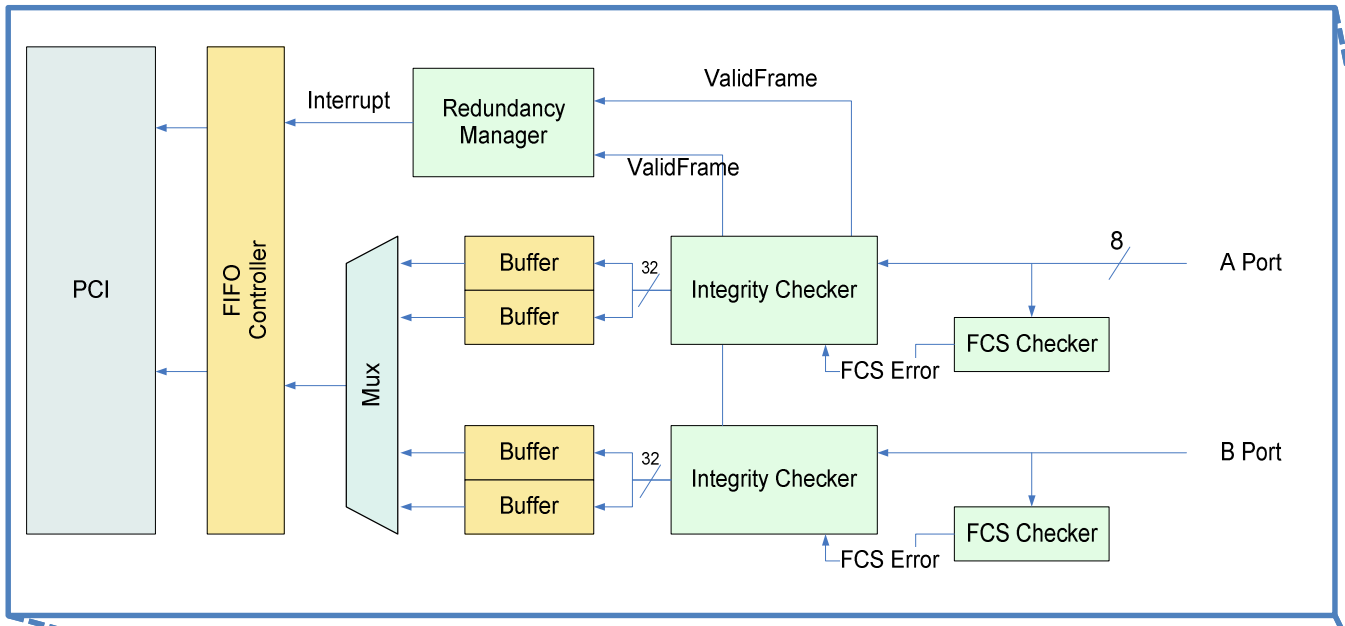


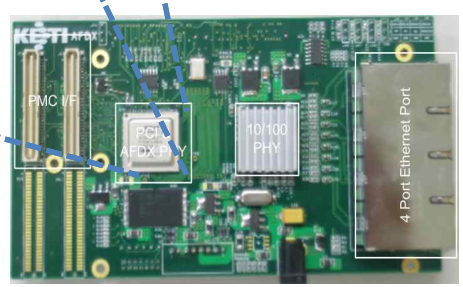


Transmission block diagram



Receiver block diagram

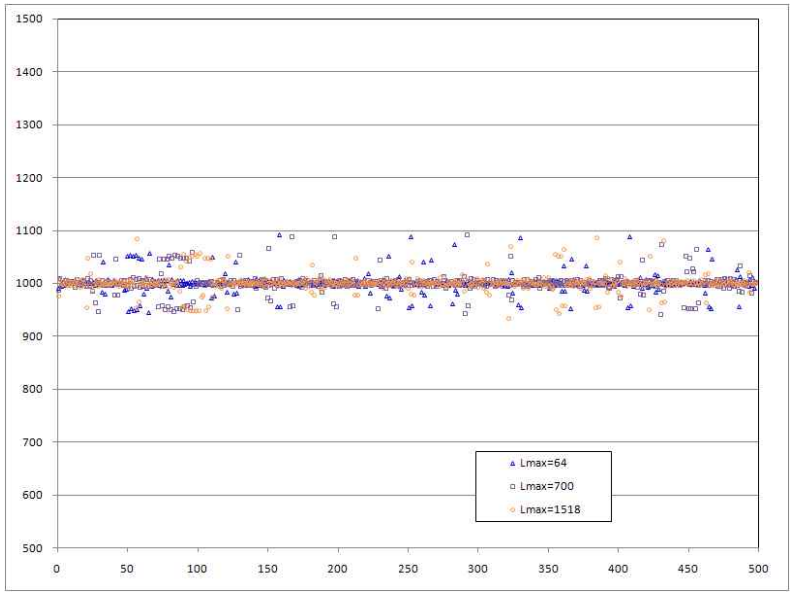


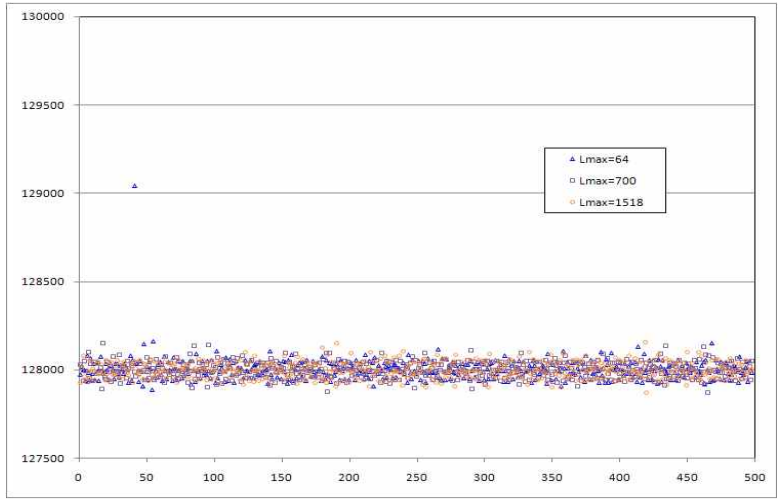


Traffic shaper's jitter performance

Software-based AFDX

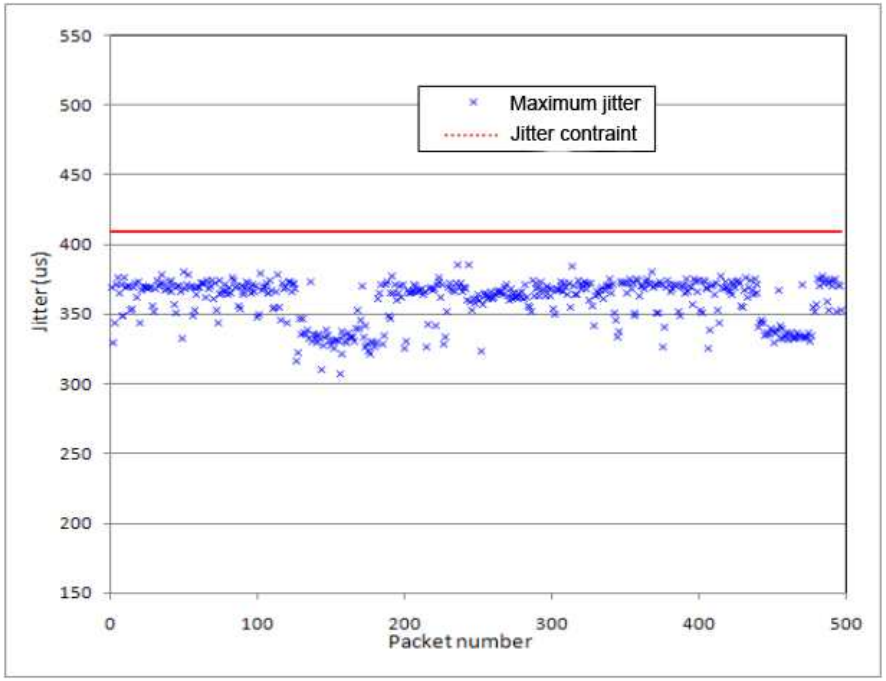
BAG [ms]	Lmax [bytes]	Max. jitter [%]	Avg. jitter [%]
1	64	9.22	0.84
	700	9.12	0.99
	1518	9.52	0.9
64	64	1.68	0.07
	700	1.63	0.08
	1518	1.64	0.08
128	64	0.88	0.04
	700	0.81	0.04
	1518	0.81	0.05





Jitter Performance evaluation

Software-based AFDX

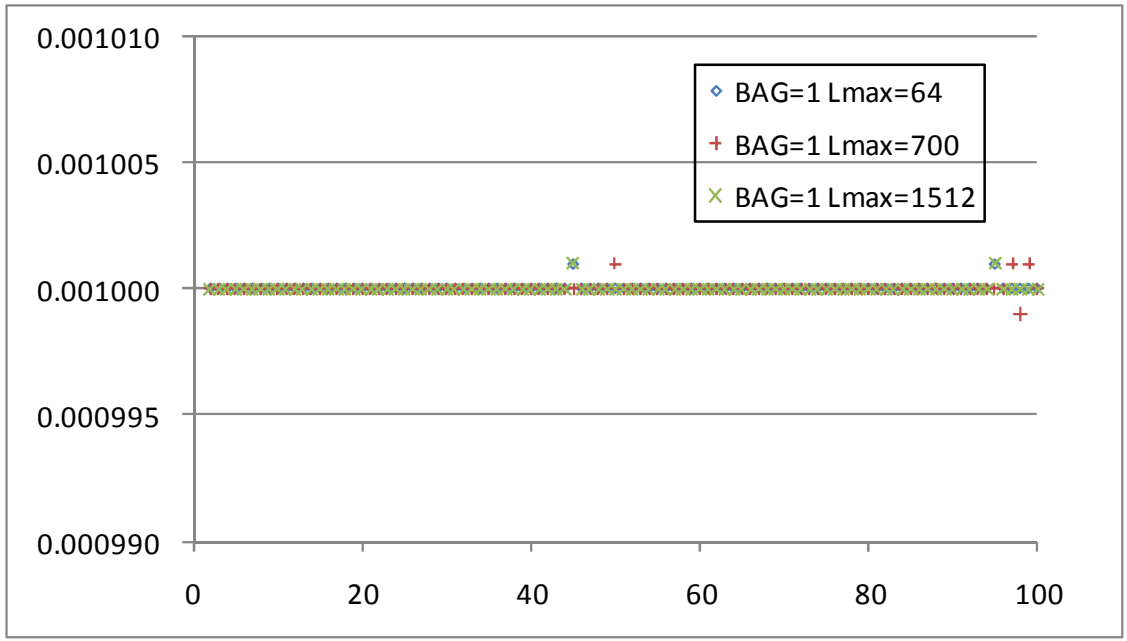


Lmax [byte]	64	700	1518
Num. of VLs	16	7	3
Max. allowable jitter [us]	147.52	443.2	409.12
Max. jitter [us]	133	691	385
Avg. jitter [us]	113.77	349.67	359.37
Success rate of jitter performance [%]	100	99.8	100

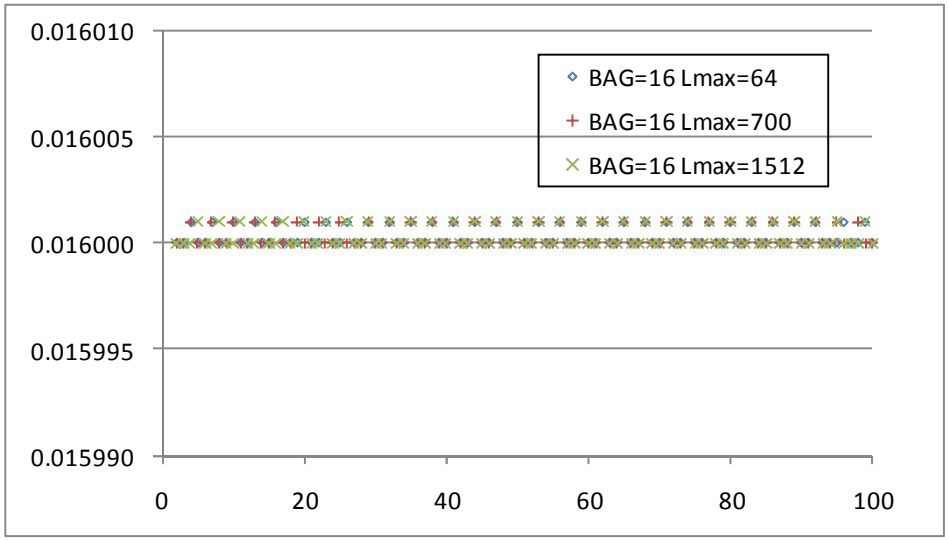
Traffic shaper's jitter performance

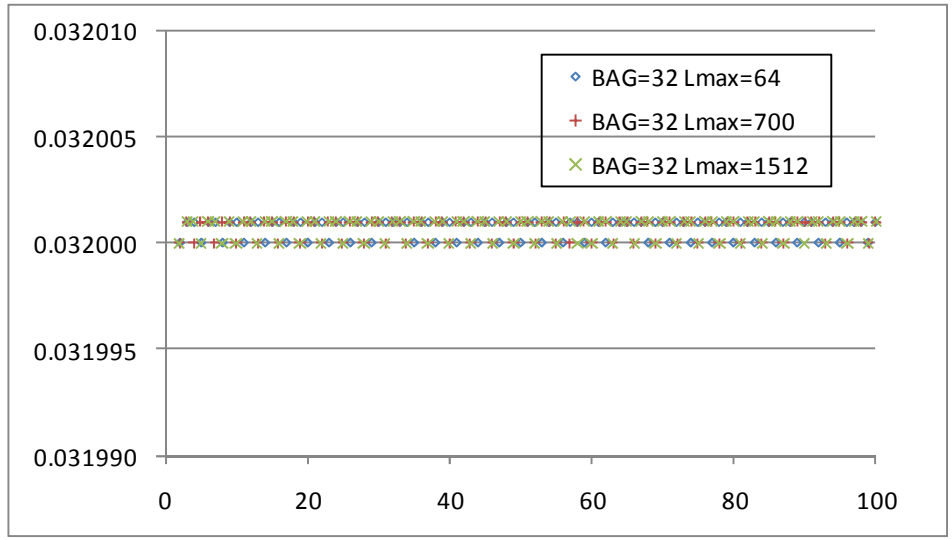
Hardwired AFDX

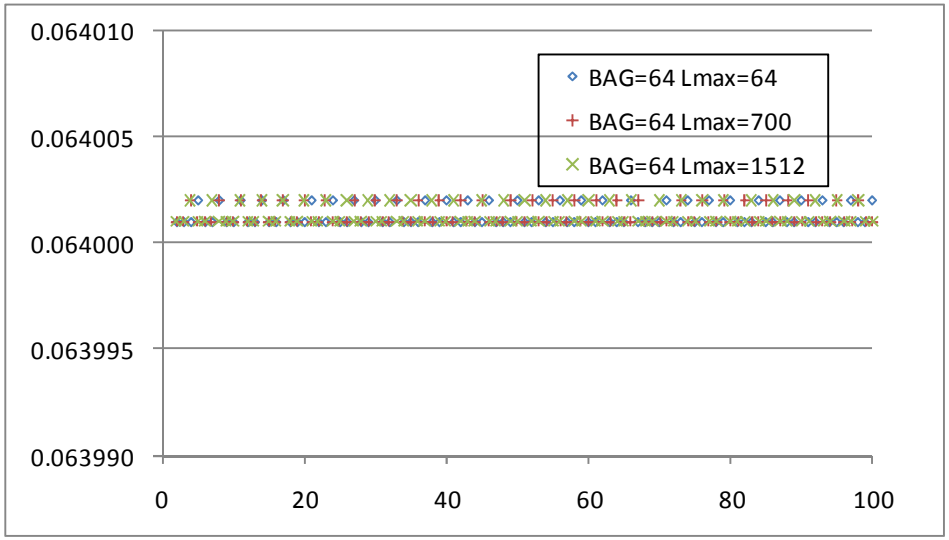
BAG (ms)	Lmax (bytes)	최대 오차율 (%)	평균 오차율 (%)
1	64	0.100%	0.002%
	700	0.100%	0.004%
	1512	0.100%	0.002%
64	64	0.003%	0.002%
	700	0.003%	0.002%
	1512	0.003%	0.002%
128	64	0.002%	0.002%
	700	0.002%	0.002%
	1512	0.002%	0.002%

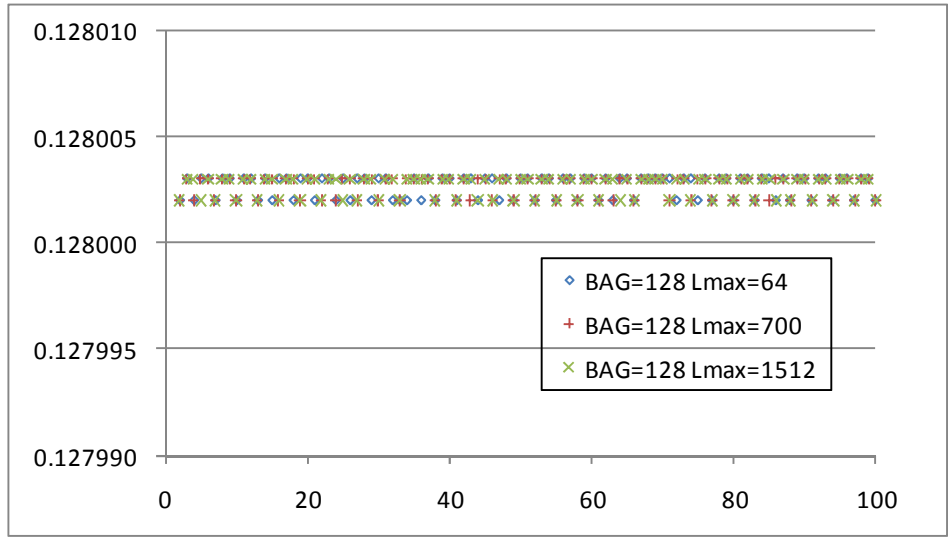


Traffic shaper's jitter performance









Conclusion

- The NetFPGA is a good reference platform at the beginning of the Project
  - PCI interconnection
  - Multiple Ethernet interfaces
- The hardwired AFDX NIC has better performance than the software-based AFDX NIC
  - Low jitter characteristics
  - Deterministic jitter

End

KETI 전자부품연구원
Korea Electronics Technology Institute